MINIMIZING THE DC-LINK CAPACITANCE OF A TWO-STAGE PV-INVERTER BY PREDICTIVE CURRENT CONTROL – INCREASING RELIABILITY AND REDUCING COST BY MEANS OF CONTROL

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ABSTRACT: The goal of this work is to reduce the DC-link capacitance of a two-stage single-phase inverter so much that the use of film capacitors becomes feasible in both, price and volume. Film capacitors instead of electrolytic capacitors could increase lifetime and reliability of the inverter, especially in high-temperature applications like module-integrated micro-inverters.

For the capacitance reduction we use predictive current control for the DC/DC and the DC/AC stage. This type of control is able to suppress a large voltage ripple at the DC-link, allowing a reduction of the installed capacitance without deteriorating the input and output current waveforms.

Keywords: Grid-Connected, Inverter, Lifetime, Photovoltaic, Reliability, Small Grid-Connected PV-Systems

1 PURPOSE AND INTRODUCTION

A lot of work has been invested into reducing the DC-link capacitance of inverters in order to replace electrolytic capacitors with the more reliable, but also more expensive and larger film capacitors. Especially single-phase inverters have a relatively high capacitance need because of the non-constant instantaneous power fed to the AC-grid which leads to a current ripple at twice the grid-frequency. This ripple current has to be delivered from the DC-link capacitor.

In low-power applications - especially for module-integrated inverters - the single-phase configuration is advantageous because of its simplicity. Different methods for reducing the capacitance needs of this configuration have been proposed [1-4]. The disadvantage of all these methods is that they require additional power switches and create additional losses, thus compromising the efficiency and cost of the system.

Our method uses a standard two-stage converter consisting of a DC/DC-input stage and a DC/AC inverter connected to the grid as shown in Fig. 1. The topology of the DC/AC-stage could also be a transformerless type, like H5 or HERIC. We used a topology with 50 Hz transformer for simplicity in the lab-setup, even though the transformerless inverter would make more sense as real application.

Compared to standard linear control, predictive Current Control (PCC) has the advantage that it is able to reject voltage variations at the DC-link very well. This means that the input- and output current of the converter are a constant DC respectively a pure sinusoidal current, even when the voltage ripple at the DC-link is high. The larger allowable voltage ripple can be used as a degree of freedom for the converter design. Especially installing a smaller capacitance at the DC-link is an interesting application of this freedom, because it makes the use of film capacitors feasible instead of the electrolytic type with lower lifetime [5]. In addition the stored energy is reduced, increasing safety in fault and short-circuit situations. Cost saving can also be achieved, if for example a large electrolytic DC-link is replaced by a smaller and cheaper one.

2 PREDICTIVE CURRENT CONTROL - METHOD

2.1 Overall control structure of the converter

Fig. 2 shows the overall control structure of the converter. PCC is used for the inner current control loops of both, DC/DC and DC/AC stage. The outer control loops (DC-link-voltage and PV-voltage) are standard PI-controllers. The outermost loop for the DC/DC-stage is a maximum power tracker.

Figure 1: Topology of our setup. Both capacitances C_in and C_DCL are to be minimized by the control strategy.

Figure 2: Control structure. The red blocks are the inner current controllers using PCC. All measurements are sampled with 100–kHz. The (white) outer control blocks are more or less standard and not the focus of this paper.

2.2 The inner current controllers with PCC

PCC is a cycle by cycle based method which is in theory able to track the current reference within one switching cycle [6-8]. Taking into account the digital implementation, where the measured quantities have to
be sampled in order to calculate a new duty cycle for the next cycle using the control law, the method tracks the reference within two switching cycles.

We implemented PCC for both, the DC/DC and the DC/AC-stage. For the design of the PCCs the converter including the sampling of the measured values and the PWM-generation has to be modeled. In general the concept is the same for both power stages: Depending on the state of the power switches, the inductor current can be described by a piece-wise linear function of input- and output-voltage and the inductance. This function is used for finding a current estimate two switching cycles ahead. The control error is calculated by subtracting the estimate from a reference. As the last step a new duty ratio which leads to zero or minimum control error is calculated. We combined the estimation and the duty-update into one compact equation which is easy to implement on a fixed-point processor.

2.3 Derivation of the control law for the DC/DC stage in more detail

The objective of the controller is to control the inductor current \( i_L \) of the boost stage. In continuous conduction mode, this current is a linear function of time. During the on-time of the power switch it has a positive slope \( m_1 = \frac{V_{in}}{L} \) and during the off time (diode conducts the current) a negative slope \( m_2 = \frac{(V_{in}-V_{out})}{L} \). (Note that \( V_{out} > V_{in} \) in a boost stage.)

After the current is sampled, these linear functions can be used to predict the current in the next sampling instant. The estimated current is a function of \( V_{in}, V_{out}, L \) and the duty ratio \( d \).

As shown in Fig. 3 we use dual-edge PWM and sampling in the middle of the rising and falling edge of the current. The blue graph is the inductor current. The sampling instants are marked by blue dots.

![Figure 3: Simulation: Tracking of a step change (current reference for DC/DC-stage is changed from 1 to 5 A). The computational delay after the step is visible. After that the current slope is only limited by the inductance. There is no overshoot. This figure is also used for explaining the principle of operation.](image)

After sampling the \( k \)-th inductor current \( I_L(k) \), the next current sample can be estimated by the function (\( T_{sw} \) is the switching period of the converter):

\[
I_{L,est}(k+1) = I_L(k) + \frac{T_{sw}}{2} \left[ d(k) \left( m_1(k) - m_2(k) \right) + m_2(k) \right]
\]

Here \( I_{L,est}(k+1) \) is the estimated current, \( I_L(k) \) the sampled inductor current, \( T_{sw} \) the switching period. \( m_1(k) \) and \( m_2(k) \) are the positive and negative slopes of the inductor current, based on the sampled voltages \( V_{in} \) and \( V_{out} \).

At the instant, when this estimation is made, the duty cycle \( d(k) \) is applied to the switches already. The next duty cycle which can be influenced by the controller is \( d(k+1) \).

Here for finding this value, first \( I_{L,est}(k+2) \) is found by estimating one step further ahead:

\[
I_{L,est}(k+2) = I_L(k) + \frac{T_{sw}}{2} \left[ d(k) + d(k+1) \right] \left[ m_1(k) - m_2(k) \right] + m_2(k)
\]

The control objective is that \( I_L \) tracks the reference current \( I_{ref} \). Therefore \( I_{L,est}(k+2) \) is substituted by \( I_{ref} \) and the equation is solved for \( d(k+1) \):

\[
d(k+1) = \frac{2[I_{ref} - I_L(k)]}{T_{sw} \left[ m_1(k) - m_2(k) \right]} - \frac{2m_2(k)}{m_1(k) - m_2(k)} + \frac{d(k)}{2}
\]

The equation is the model predictive control law for controlling the DC/DC stage.

The derivation for the DC/AC-stage is analog and very similar. Here we only show the result:

\[
d(k) = \frac{2[I_{ref,AC} - I_L(k)]}{T_{sw} \left[ m_{up} - m_{down} \right]} - \frac{2m_{down}}{m_{up} - m_{down}} + \frac{d(k)}{2}
\]

Where \( I_{L,AC} \) is the sampled inductor current, \( I_{ref,AC} \) the reference current and \( T_{sw} \) the switching period. \( m_{up} \) and \( m_{down} \) are the positive and negative slopes of the inductor current:

\[ m_{up} = \frac{(V_{DCL} - V_{AC})}{L_{AC}} \quad \text{and} \quad m_{down} = \frac{(-V_{DCL} + V_{AC})}{L_{AC}}. \]

4 EXPERIMENTAL RESULTS

For experimental verification we used a small-scale setup with a topology like shown in Fig. 1. It has a nominal DC-link voltage of 25 V and is connected to the grid via a 12V/230V transformer. It is controlled with a 320F2808 DSP from Texas Instruments. This is a fixed point DSP, running at a clock frequency of 100 MHz. A photo of the board is shown in Fig. 4.

For the experiments we started with a DC-link capacitance of 4 mF which corresponds to a stored energy of 18 Ws/kW. The input filter capacitance was initially 2 mF. During the experiments we reduced the DC-link capacitance to 1 mF and the input capacitance to 100 µF. A further reduction is possible, but for time reasons we stopped at that point.

![Figure 4: Photo of the experimental board.](image)

A first result is shown in Fig. 5. It shows the tracking of a step change of the reference current for the DC/DC-stage. It looks very much like the simulation in Fig. 3. The reference current is tracked after a short
computational delay. When the reference is reached, there is no overshoot. Note that the (blue) reference signal is not to scale to the current. The step was from 1 to 5 A.

Fig. 6 shows the input and output waveforms of the complete converter setup in closed loop control and with reduced capacitance. As a consequence, the ripple at the DC-link is large (33% of the rated DC-link voltage of 25–V). This ripple is suppressed nicely and not visible in either the input voltage or output current of the converter.

For comparison, we also operated the setup with classic PI control for the inner currents loops. The result is shown in Fig. 7. The ripple at the DC-link is the same, but the input voltage shows a significant ripple. This ripple would have to be removed by a larger input filter to avoid power loss due to the fluctuating operating point of the PV-generator.

**Figure 6:** Input and output current and voltage with PCC and reduced capacitance. Even though the voltage ripple at the DC-link is 10 Vpp (33% Ripple), the PV-voltage is constant.

**Figure 7:** For comparison: Input and output current and voltage with classic PI/PR-control and reduced capacitance. There is a considerable ripple at the PV-input, leading to energy loss because of non constant working point within the PV-characteristic.

5 CONCLUSION

The high performance of PCC allows replacing electrolytic capacitors with film capacitors which are more reliable and temperature stable. No additional hardware is needed, thus the efficiency is not reduced by additional stages processing the power.

Another advantage is that the controllers do not need tuning. There are no adjustable gains like in linear control. This saves development cost and makes the control easily scalable.

We tested the controllers both in simulation and experiments on a small-scale setup. The large voltage ripple at the DC-link is suppressed on both input and output current of the converter. The grid current has very low harmonic content. This makes the use of film capacitors possible without increasing the volume of the device.

6 REFERENCES


