A Performance Analysis of Three Potential Control Network for Monitoring and Control in Power Electronics Converter

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Abstract—A simple and fast internal communication system is highly demanded for future complex Power Electronics (PE) converters such as multilevel converters. To increase the reliability, more data/information will be required for local/internal monitoring and control. Therefore, a high speed control network is essential for the future PE converter system. This paper will first present the basic communication requirements for future advanced control in PE converters. Three potential high speed (100 Mbps) control networks (MACRO, PROFINET IRT, and EtherCAT) are being reviewed and analyzed. Finally, a case study is presented on a 3 phase Modular Multilevel Converter.

I. INTRODUCTION

The concept of Electronic Power Distribution System (EPDS) had been proposed for the future smart grid. The goal is to reduce the complexity, cost and power loss. On the other hand a reliable local power distribution system is believed to consist of multiple energy sources and back-up energy storages. Therefore, different range of Power Electronics (PE) converters will become highly demanded [1]. It is believed that standardizing the PE converter design will be actively discussed in order to realize EPDS (Smart Grid).

The design process of PE converter can be simplified with the concept of Power Electronic Building Block (PEBB). The goal of PEBB is to cover a wide range of power conversion applications with a set of power electronics blocks that can operate together [2, 3]. A PEBB is fully integrated with low level protections, gate drivers, measurement sensors and communication interfaces. It is a platform based design with open plug and play architecture. The system must be intelligent enough to automatically identify each component and manage to self-configuring [4]. The concept of PEBB has been developed and analysed in ship application. It is believed that PEBB will be the future trend of shipboard systems [5] as well as the future smart grid. Fig. 1 shows functional decomposition of a PEBB [4].

The key functional component for PEBB is the power electronics controller, where Digital Signal Processor (DSP) or FPGA are commonly used. The conventional control interface between the controller and the gate drivers is realized by a star topology. A number of wires are usually needed for the switch commands, fault signals, and all the sensor measurements (voltages, currents, temperature). An estimation of lines versus different three-phase power converter topologies had proved that the need of wires will increase drastically for a complex system [6]. The root cause of this is the star topology only supports one way communication. Undeniable, a power converter with high number of wires will increase the cost and noise problem. Therefore, a simpler wiring system is highly demanded for future PE system.

This paper will first formulate the basic communication requirements for future advanced control in PE converters and then investigate the potential control networks which support high speed local/internal monitoring and control of the power electronics system designed. The rest of this paper is organized as follows. Section II introduces the communication requirements. Section III proposes and briefly reviews three potential control networks. An overview on performance evaluation in PE converter system is presented in Section IV and the minimum cycle time analysis and comparison among the three potential control networks will be outlined in Section V. Finally, a case study is presented in Section VI and conclusion is given in Section VII.

II. COMMUNICATION REQUIREMENTS FOR MONITORING AND CONTROL IN PE CONVERTER

A. Network Topology

Ring topology seems to be most applicable for future needs due to its simplicity in wiring and low cost. Ring network is set up in a circular form where data travels around the ring in one direction, either clockwise or counter clockwise. The data transmitting to and from the nodes in the power converter...
system are short. The switch commands, fault signals, and all the measured variables can be formulated in packet formats and sent at a constant rate throughout the ring in series. Fig. 2 shows the structure of star and ring topology [6-9].

B. Transmission Medium and Link Length

Power converters normally operate at a noisy environment which involves numerous transitions between high and low energy. Hence, optical fibers are preferable. Since, they are immune to electromagnetic interference and promise high speed transmission. With ring topology, the maximum length is predicted not more than 30 meters within the converter, even with multilevel converter.

C. Communication Mode

A conventional power converter control system operates in Master-Slave communication mode. A controller acts as a master where the sampled data are being processed and the next control signals for the power switches are determined. The control signals are then send to each phase leg of the power switches, which are recognized as slaves. Future PE converter may include redundancy control to increase the system reliability. A backup controller and some additional standby devices will be placed in the system; hence Master-Master or peer-peer communication mode should be reserved for future development.

D. Synchronization

Although Ring topology simplified the wiring of a power converter system, however a propagation delay is formed when data transmit from nodes to nodes. Therefore, synchronization of the switching for each phase leg is essential. Asynchronous behaviour of phase legs will increase the current and voltage ripples. It may also cause a catastrophic failure if the operation of converter is totally out of synchronism.

E. Communication Network Nodes

A communication network node in PE converter system is equivalent to a unit of PEBB. A PEBB can be based on a single power switch, or a few power switches integrated in half-bridge, or H-bridge modules. By assigning an address, the PEBB will be able to communicate in a ring by transmitting and receiving data packets. Ideally a PEBB is standard, re-useable and replaceable. A simple three phase system may employ 4 network nodes, a master node (controller) and 3 slave nodes (PEBB is defined as 2 power switches in half-bridge module). However, a complex system may contain a large amount of slave nodes (PEBB) such as multilevel converter. Assume the total number of network nodes in a complex system should not more than 33 nodes.

F. Bandwidth

Data exchange between nodes within a power converter may include the values of voltage, current, status, and switching duty ratio. These data may be sampled at regular interval. The required data bandwidth in power converter system can be estimated using the following equation:

\[
\text{Bandwidth} = N_{\text{var/node}} \times n_n \times n_b \times f_{sw} \times (1 + k_{oh})
\]  

(1)

\[N_{\text{var/node}} : \text{Number of variables per node}
\]  

\[n_n : \text{Number of nodes in the system}
\]  

\[n_b : \text{Resolution of PWM signal sent from the controller to the nodes}
\]  

\[f_{sw} : \text{Switching frequency of the power converter}
\]  

\[k_{oh} : \text{Percentage of data overhead, which needs to be transmitted along with the data}
\]

The number of variables per node, \(N_{\text{var/node}}\), is basically defined as four. The resolution of PWM signal sent from the controller to the node, \(n_b\), is proposed to set at minimum 10 bits in order to ensure sufficient time resolution within 1 switching period. It is believed that tiny step time is more flexible for nodes synchronization. Switching frequency of the power converter is assumed to set as 10 kHz (typical value). By assuming 50% data overhead, the minimum bandwidth of the proposed system could be estimated using (1).

\[
\text{Bandwidth} = N_{\text{var/node}} \times n_n \times n_b \times f_{sw} \times (1 + k_{oh})
\]

\[= 4 \times 3 \times 10 \times 10000 \times (1 + 0.5)
\]

\[= 1.8 \text{Mb/s}
\]

Higher bandwidth will be required for a complex system as the bandwidth is proportional to all the variables. The desired bandwidth for this research is set to approximately 100 Mb/s to allow more flexibility in the system design and for future expansion. Table I summarized the basic requirements for monitoring and control in PE converter.

III. CONTROL NETWORKS

Three potential control networks (MACRO, PROFINET IRT and EtherCAT) with broad bandwidth range above 100 Mbps are briefly reviewed. Their basic characteristics are summarized in Table II [10-14].

A. Motion and Control Ring Optical (MACRO)

MACRO is developed by Delta Tau Data Systems for connection of multi-axis motion controllers, amplifiers, and I/O. The Virginia Polytechnic research team had developed Power Electronics System Network (PESNet) based on MACRO protocol in 1999. PESNet is a custom-made solution in PE converter systems for data exchange control.
between a power stage and a digital controller. The following paper will focus on the analysis of PESNet.

B. PROFINET IRT

PROFINET IRT is mainly developed by Siemens. It reduces the cycle times in the range of a few microseconds to 1 millisecond with maximum precision. PROFINET offers a series of special functions. Among all, isochronous data transmission for high-accuracy closed-loop control tasks and redundancy concept in PROFINET IRT are the most attractive features in PE converter system. PROFINET IRT requires special hardware support (ASIC) on both master-slave devices [11].

C. EtherCAT

EtherCAT is a single large Ethernet device, defined by Beckhoff. It is mainly developed for maximum efficiency and short cycle times [13]. The incoming telegrams are directly being process and extract the relevant data or insert new data and transmit to the next slave. The last slave will forward back the fully processed telegram to the master in full duplex mode. EtherCAT provides accurate diagnostic on faults detection, standard Ethernet checksum and distributed clocks with a jitter of significantly less than 1 µs [14].

IV. PERFORMANCE EVALUATION IN PE CONVERTER SYSTEM

The cycle time, $T_c$ is defined as the time necessary to exchange the input/output data between the master controller and all slave devices once [15].

$$T_c = T_{tx_Do} + T_{Processing} + T_{tx_Do} + T_{Idle}$$

Where $T_{tx_Do}$ is the time taken by the master to transmit the computed output data to the corresponding slave nodes, $T_{Processing}$ is the time taken by the master to process input data and compute output data, $T_{tx_Do}$ is the time interval for the system to remain inactive between subsequent cycles.

While minimum cycle time is defined as to elapse between two consecutive executions of one cyclic action (i.e. reading/writing of data from/to a network node) and can thus be defined as the minimum sampling time achieved by the network system [16].

$$T_{min} = T_c + T_{Processing} + T_{Idle}$$

The cycle time analysis will be demonstrated based on a simple three phase PE converter system as shown in Fig. 3. A high speed controller is employed; assume that the data processing time is less than 100 µs. Data packet for the last node is programmed to be transmitted first in order to minimize the cycle time [15]. Data packets are transmitted continuously in counter clockwise direction with no inactivity (Idle) time is considered. Fig. 4 shows the ideal timing diagram of the cycle time analysis.

As all the states variables is sampled at $t_0$, the data can then be packed into the appropriate data frame and started forwarding from node to node at $t_1$. By assuming that the data packet is transmitted one after another and the period to transmit a data packet from a node to its neighbour node is define as $T_{fwd}$. Hence, all the data should be able to reach the controller after four $T_{fwd}$ intervals at $t_2$. After a period of processing time, output data can be packed and transmitted to the corresponding nodes start from $t_3$ to $t_4$. In order to achieve a synchronization operation, all power switches can be activated at/after $t_5$. The system can be optimized by having back-to-back data processing with the input data is sampled before the end of the data processing cycle (Fig. 5).

![Fig. 3. 3-phase PE converter with a controller (master node) and three PEBB (slave nodes)](image)

![Fig. 4. Timing diagram analysis for one cycle](image)

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$T_{tx_Do}$ : Total time taken by the slave nodes in a system to transmit its data to the master over the network.

$T_{Processing}$ : Time taken by the master to process input data and compute output data.

$T_{tx_Do}$ : Total time taken by the master to transmit the computed output data to the corresponding slave nodes

$T_{Idle}$ : Time interval for the system to remain inactive between subsequent cycles.

Where $T_{tx} = T_{tx_Do} + T_{Processing} + T_{Idle}$ (3)
Fig. 5. Cycle time minimization for simple system in Fig. 3, using back-to-back data processing

The processing time, $T_{\text{Processing}}$, varies due to different PE converter controlled algorithms and the speed of the processor. It does not depend specifically on the communication protocol (control network), therefore it will be neglected in order to simplify the minimum cycle time analysis. Equation (3) can then be simplified as (4) by eliminating the idle time as well.

$$T_{\text{cm}} = T_a$$

$T_a$ represents the total time taken to forward a data packet from node to node with some propagation delay. It is formulated differently based on different characteristics of a control network.

V. MINIMUM CYCLE TIME ANALYSIS AND COMPARISON FOR PESNET, PROFINET IRT AND EtherCAT

Overview on the definition of minimum cycle time for each control network will first be presented, followed by the worst case minimum cycle time estimation in a complex PE converter system. Assume that a complex system contains a master and 32 slave nodes. The nodes are physically placed close to each other; assume not more than 0.3 m. The common exchanged data in PE converter system are short, therefore the following analysis will limit the data payload to a range of 4-Byte (minimum) to 10-Byte (maximum). Data Frame Format for each control network is fully described in its specification [10, 13, 17].

A. PESNet

The cycle time of PESNet mainly depends on three factors; (i) the number of data packets sent per ring cycle (equals to the number of active nodes), (ii) the number of stations on the ring, each with a transceiver delay and (iii) the length of the conductors between stations allowing for the speed of light (fiber system).

PESNet is designed to communicate at a fixed frequency. The transmission rate is 125 Mbps. The protocol of each transmission occurs as 4B/5B (ANSI X3T9.5 FDDI) coded data. Each actual byte is transmitted as 10 bits (8 data bits + 2 redundant bits) [10]. Based on this definition, the $T_{\text{fwd}}$ can be formulated as

$$T_{\text{fwd}} = \frac{n_{\text{max}} \times 10b}{125 \text{Mbps}}$$

By default, PESNet is implemented with the communication frequency defined as 500 kHz ($T_{\text{fwd}} = 2 \mu s$). PESNet 2.2 introduced flexible frame, i.e. Full Mode (FM) and Reduced Mode (RM) [18]. FM reserves 10-Byte data payload while RM limits the data payload to 4-Byte in a single packet. With some data overhead, the total length per packet for FM is 27-Byte and RM is summed up to 14-Byte. RM is recommended to transfer less information for a complex system (with more slave devices or when high switching frequency is required.)

A packet encounters a delay in passing through each node. The data is first de-serialized and then evaluated for an address match. Typical delays are 0.5 – 0.6 µs per node.

Data transmission is delayed by the speed of electromagnetic radiation in the fiber conductor. This speed is about 0.004 µs meter in fiber. This is not a significant factor in limiting the ring update rate. Therefore, the $T_{\text{cm}}$ can be formulated as

$$T_{\text{cm}} = T_{\text{fwd}} \times \left( \text{Number of active nodes} \right) + 0.6 \mu \text{sec} \times \left( \text{Number of slaves} \right) + 0.004 \mu \text{sec} \times \left( \text{total meters of conductors} \right)$$

In order to estimate the worst case $T_{\text{cm}}$, $T_{\text{fwd}}$ for FM and RM are first determined using (5).

$$T_{\text{fwd, FM}} = \frac{27 \times 10b}{125 \text{Mbps}} = 21.6 \mu \text{sec} = 2.5 \mu \text{s}$$

$$T_{\text{fwd, RM}} = \frac{14 \times 10b}{125 \text{Mbps}} = 1.12 \mu \text{sec} = 2 \mu \text{s}$$

It is believed that the PESNet 2.2 with fault tolerance [18] will have to increase the $T_{\text{fwd}}$ for FM operation (assume 2.5 µs for the $T_{\text{cm}}$ estimation). Whereas the RM operation can still remain the default communication frequency of 500 kHz.

$$T_{\text{cm, FM}} = 2.5 \mu \text{s} \times 32 + 0.6 \mu \text{s} \times 32 + 0.004 \mu \text{s} \times (0.3 \times 33) = 101.74 \mu \text{s}$$

$$T_{\text{cm, RM}} = 2 \mu \text{s} \times 32 + 0.6 \mu \text{s} \times 32 + 0.004 \mu \text{s} \times (0.3 \times 33) = 85.24 \mu \text{s}$$

B. PROFINET IRT

Isochronous Real Time communication in PROFINET is designed to follow a fixed communication schedule for each node that is repeated periodically. Although the PROFINET IRT support full duplex mode with high bandwidth 100Mbps, the system may fail if each devices keep sending data frames in this speed [19].

Every Transmission cycle contains two channels as drawn in Fig. 6 [17]. IRT channel is reserved for the transmission of synchronization frame (Sync) and isochronous real time frame (IRT). Open channel is used to transmit cyclic real-time frames (RTC), acyclic real time frames (RTA) and non-real-time frame (NRT). The send clock time, $t_{\text{send, clock}}$, represent the time interval at which all different type of data frames are sent in a transmission cycle.

Both the controller board and slave devices will take turn to act as a Provider and Consumer during data exchanged (Table II). The controller will act as a Consumer when it receives the input data from the slave devices for processing.
However, it will act as a Provider when it ready to send out data to all the slave devices. Consumer will always send back Consumer Status to the provider following of the receipt of data as an indication of complete data exchanged. A complete data exchanged between a provider and consumer will need a send clock time, \( t_{send\_clock} \).

The send clock time, \( t_{send\_clock} \) is usually programmed by the user during configuration. It is defined as

\[
 t_{send\_clock} = n \times 31.25\mu s 
\]  

(7)

where

- \( n \) : the send clock factor range from 1 to 128
- 31.25\( \mu \)s : the basic time unit.

Deriving this equation, the \( t_{send\_clock} \) should range from 31.25 \( \mu \)s to 4 ms. However, in the real implementation, the achievable minimum \( t_{send\_clock} \) is 250 \( \mu \)s, where \( n \) is limited to 8. The reason behind this limitation is to introduce a safety margin to restrict the usable portion of the cycle as 60% of the total cycle time; where the time for RT frames, \( t_{RT} \) should not exceed 50% of the bandwidth for each cycle. Consequently, the time for acyclic real-time frames, \( t_{RTA} \) should not exceed 10% of the bandwidth. The NRT frames will be sent during the rest of the available time [20].

Since the PROFINET IRT runs in a fixed communication schedule with the achievable minimum \( t_{send\_clock} \) is 250 \( \mu \)s, the worst case \( T_{min} \) estimation can be simplified as

\[
 T_{min} = n \times (t_{send\_clock} + t_{pass\_through})
\]  

(8)

Where

- \( n \) : Overall number of PROFINET IRT devices (master and slave devices)
- \( t_{pass\_through} \) : The forwarding delay of a PROFINET IRT slave, approximately 3\( \mu \)s/device. [12]

It is believed that 250 \( \mu \)s is large enough to transmit either 4-Byte data or 10-Byte data. Thus,

\[
 T_{min\_10\_B/4\_B} = (1 + 32)(250 + 3) \mu s = 8349 \mu s
\]

C. EtherCAT

EtherCAT offers an attractive advantage so-called summation frame, where data for all slave nodes can be packed into one single frame for real-time data exchange. The output data to the slave sent by the controller will be replaced by the input data of the slave on the fly. The minimum cycle time (\( T_{min} \)) in EtherCAT is formulated as a summation of frame time (\( T_F \)) and propagation delay time (\( T_P \)) [21].

\[
 T_{min} = T_F + T_P
\]  

(9)

Where

- \( T_F \) : Time taken by the master to send all the bits that make up the EtherCAT frame over the network.
- \( T_P \) : Time taken by a frame to travel across all the slave nodes in the network and come back to the master.

The frame time depends directly on the size of the EtherCAT frame and it is formulated as

\[
 T_F = s_{eth} + s_{frame} + s_{frame} + s_{IFG} \sum_{j=1}^{n} T_{EBj}
\]  

(10)

Where

- \( n \) : Number of the EtherCAT telegrams included in the Ethernet frame
- \( s_{eth} \) : Size of the frame protocol control information in total 28 bytes. (26-Byte: Ethernet preamble, destination and source address, ethertype and CRC; 2-Byte: EtherCAT frame header.)
- \( s_{frame} \) : Size of the telegram protocol control information in total 12 bytes. (2-byte: header and WKC.)
- \( T_{byt} \) : The transmission time of 1-byte. (80 ns in currently available 100 Mb/s networks)
- \( s_{IFG} \) : Size of the inter frame gap in total of 12 bytes.

The number of slave devices directly affect the frame time. The higher the number of devices hook up to the network meaning that the larger the amount of information that has to be exchanged between the master and slaves, which indicates that a longer duration for \( T_F \) will be needed.

In ring topology, every frame sent by the master will travel around the whole network before being received again by the master on the return path. Therefore, the overall propagation delay \( T_P \) is defined based on the number of connected devices and the network extension.

\[
 T_P = \sum_{j=1}^{n} (T_{ETj} + \tau_e \cdot L_{ETj}) + \sum_{j=1}^{n} T_{EBj}
\]  

(11)

Where

- \( n \) : Overall number of Ethernet devices (master and slave devices) in the system (including couplers to EBUS segments)
- \( T_{ETj} \) : Pass through delay of the \( j \)th Ethernet devices. (typical value 1 \( \mu \)s or less)
- \( L_{ETj} \) : Length of the Ethernet cable connecting it to the previous node.
- \( \tau_e \) : Specific propagation delay (~10 ns/m)
- \( n_{EB} \) : Overall number of devices connected through EBUS backplanes
- \( T_{EBj} \) : The pass through delay of the \( j \)th EBUS device. (typical value 60 ns)

Pass-through delay is mainly affected by the physical transceivers adopted; namely plain Ethernet and EBUS. The former solution means for connecting separate devices using fiber optics, whereas the latter is intended to be used as a low-cost backplane for modular devices attached to a mounting rail (EBUS is not qualified for wire connections). Assume PE converter will not implement in EBUS, hence, \( T_{EBj} = 0 \).

By using (9), (10) and (11), the worst case \( T_{min} \) can be calculated as followed.
system in future advanced PE converter followed by outlining a set of basic requirements for selecting a potential control network. Performance analysis for three potential control networks (PESNet (MACRO), PROFINET IRT and EtherCAT) has fully described and compared. In addition, a specified Modular Multilevel Converter (M2C) had been investigated. The result shows that a control network with fixed communication schedule like PROFINET IRT is not suitable in PE converter system. The length of data payload and the number of communication nodes specify the regular communication bandwidth.

VI. CASE STUDY – MODULAR MULTILEVEL CONVERTER

Modular Multilevel Converter (M2C) offers some superior features compared to the conventional multilevel converter [22]. It is believed that M2C is one of the good solutions for future EPDS with its modular concept. Hence, a three-phase M2C is chose to further examine the three potential control networks.

In this study, a three-phase M2C limited to six PEBB per phase. Each PEBB is defined as two power switches in half-bridge topology. A ring network topology is adopted for each phase. There is one master controller taking care of all the ring communication. The length of each ring is about 2 m (distance between two neighbor nodes is less than 0.3 m). Data payload is limited to 4-Byte per packet. Each slave node will transmit two sets of sensing variables (together with some status bits) to the master controller. The data sampling rate is set at 10 kHz. The master controller will send the corresponding switching command (modulation information) with synchronization signal to the appropriate slave node. The six PEBB within a ring must be synchronized with a time resolution less than 500 ns (time between the first and the last PEBB). The \( T_{\text{Cmin}} \) for the three potential control networks can be estimated for this study case by using equation (5) – (11). Results are given in Table III.

PROFINET IRT fails to achieve 10 kHz data sampling rate. So PESNet and EtherCAT are more preferable for this study.

VII. CONCLUSION

This paper has discussed the need of a communication

| TABLE III | THE MINIMUM CYCLE TIME (\( T_{\text{Cmin}} \)) SUMMARY FOR WORST CASE ESTIMATION AND MODULAR MULTILEVEL CONVERTER (M2C) |
|---|---|---|---|
| \( T_{\text{Cmin}} \) | PESNet | PROFINET IRT | EtherCAT |
| Worst Case | \( T_{\text{Cmin,wb}} \) | 101.74 \( \mu \)s | 8349 \( \mu \)s | 92.62 \( \mu \)s |
| | \( T_{\text{Cmin,ad}} \) | 85.24 \( \mu \)s | 8349 \( \mu \)s | 77.26 \( \mu \)s |
| M2C | \( T_{\text{Cmin}} \) | 17.61 \( \mu \)s | 1771 \( \mu \)s | 17.90 \( \mu \)s |

References


