Ride-Through Enhancement of Line-Commutated HVDC Link for Large Offshore Wind Parks

Muhammad Jafar, Marta Molinas
Norwegian University of Science & Technology, Trondheim, Norway
muhammad.jafar@elkraft.ntnu.no, marta.molinas@elkraft.ntnu.no

Abstract—The CIGRE benchmark model for HVDC has been tested for post-fault commutation failures. The observation of the phenomena of post-fault commutation failures and large oscillations in currents and voltages at the inverter and rectifier terminals is explained. These oscillations lead to further commutation failures during recovery and increase the recovery time after original fault clearance. A detailed investigation of control instability is carried out and the components of the control system behaving against expectation are identified. Control modifications are suggested and compared to the control system in the example case in PSCAD®/EMTDC. Simulation results are presented and compared with the standard case, which indicate that the suggested control structure exhibits improvements in inverter DC current dynamics to eliminate the risk of post-fault commutation failures due to fault occurrence and clearance at inverter ac bus.

Index Terms—Power Electronics, Power Electronic Converters, High-Voltage and Multilevel Converters

I. INTRODUCTION

The importance of HVDC transmission in case of large offshore wind-farms is evident as future offshore plants will be quite far from the coasts making it impractically expensive to employ HVAC in those circumstances [1]. The MVA ratings of future offshore plants [2] may be much larger than the current power handling capacities of Voltage Source Converter based HVDC (VSC HVDC) transmission technology [3]. This leaves Line Commutated Converter based HVDC (LCC HVDC) transmission technology [4] as the only viable option to be employed in this scenario.

There are, however, certain inherent problems that make LCC technology vulnerable and one of these is the commutation failures [5]. A Commutation failure is a failure of current to transfer from one conducting thyristor to the other. The consequence of this is that a short-circuit is placed across the converter pole undergoing commutation failures reducing the DC voltage of that converter to zero. During commutation failures, no power is converted from ac to dc on the rectifier side of the link and none from dc to ac on the inverter side. The other effects are the current and voltage stresses on the thyristor switches as well. Repeated occurrences of commutation failure will force the control to shutdown the link.

The inverter terminal of any HVDC link is more prone to this problem when compared to the rectifier terminal. Commutation failures are experienced when there is not enough time for the outgoing thyristor to de-ionize due to insufficient commutation margin (This margin is quite high in case of rectifier terminal). The reduction in commutation margin may be caused by a reduction in commutating voltage, a negative phase shift in the commutating voltage, an increased commutating current, or a combination of these [6]. This has to be noted that to achieve the maximum benefit out of the DC link, rectifier terminal operates near the minimum firing delay angle and the inverter terminal operates at a minimum extinction angle. This has the added benefit of minimum reactive power consumption possible [5].

Commutation failures may occur at the inception of a disturbance [6] and also during recovery from a disturbance [7]. In both these instances, these are highly undesirable as they disturb the normal operation of the link. In the latter case, these failures increase the recovery time of the link reducing the ride-through capability of the link.

Many accounts of commutation failures are available in literature but almost all of them treat the instance at the inception of fault and not during recovery after fault. There are some papers that address the issue [7, 8], but not in great detail. The authors have also worked on the topic in a recent publication [9] where the issue is resolved but the detailed modelling and mathematical foundation is not provided.

This work focuses on prevention of post-fault commutation failures. The methodology is to analyze the DC system dynamics of the first CIGRE benchmark for HVDC studies [10] which is modelled as an example case in PSCAD®. First, the existing model is simulated with a three-phase fault on the inverter bus and its effects are analyzed. Different parameters of the control are observed for compliance to different requirements for quick recovery. A discrepancy is identified and explained causing the mal-operation during recovery from faults. Based on the analysis, a variation in control of firing angle is suggested and simulations have been carried out to verify that the suggested control scheme reduces the risk of commutation failures after fault removal reducing recovery time and in the process enhancing the ride-through capability of the system.

II. PROBLEM DESCRIPTION

The CIGRE benchmark model consists of a 12-pulse single pole configuration. The rated DC link voltage is 500 kV and...
the rated DC current is 2 kA. The transmission line is modelled as a T-section with the shunt line capacitance lumped at the mid-point and half of the series impedance lumped in each half. This series impedance contains the series connected current smoothing inductance as well. The rectifier and inverter ac sides are equipped with filters and power factor correction capacitors. The AC sources forming part of this benchmark model have a short-circuit ratio (SCR) equal to 2.5 signifying weak systems feeding the link as well as being fed by the link.

The model is simulated with a three-phase to ground fault at the inverter bus occurring at 1 s. The duration of the fault is 100 ms. Inverter and rectifier DC currents are plotted in Fig. 1 and Fig. 2 respectively. The currents magnitudes have been per-unitized on the base value of 2 kA. The fault is cleared at 1.1 s, but as soon as the recovery process starts, the currents at both the terminals first increase a little, then go down, shoot up once again to high values, reducing to minimum values once again before recovering again. These oscillations delay the recovery till almost 1.5 s which is approximately 0.4 s after the clearance of the fault.

Fig. 2 also shows the current order for rectifier which dictates the firing delay angle (α) for rectifier. This current order is controlled by the inverter DC voltage and current. The rising DC voltage and current at the inverter terminal are responsible for a rise in the current order shortly after fault clearance.

Fig. 3 and Fig. 4 show the DC voltages at the rectifier and inverter terminals respectively during the same period after being per-unitized on the base value of 500 kV. It is evident that inverter current shoots up as soon as the DC voltage goes down at the inception of the fault. The dropping voltage reduces the reference current for rectifier using Voltage Dependant Current Order Limit (VDCOL) which takes corrective action to reduce the current to a lower level (0.55 pu in this case). The difference between the oscillations in rectifier and inverter currents is quite striking. Inverter current exhibits a more oscillatory behaviour than the rectifier current due to effect of line capacitance. Upon clearance of the fault, DC voltages start to rise but at a specific time inverter DC voltage goes down again (due to short-circuits caused by commutation failures) taking down the current order and the rectifier DC voltage. The system recovers in the second effort after this failure.

Fig. 5 shows the α-orders for rectifier and inverter terminals. The extinction angle (γ) for inverter terminal is plotted in Fig. 6.

A thorough examination of Fig. 1 through Fig. 6 reveals the critical moments after fault clearance. As soon as the fault is cleared, a voltage without any control action is introduced in the path of the inverter current (Fig. 3). In this case this voltage is opposing the inverter current and hence it drops to almost zero, without any change in current order or the firing delay angle (Fig. 1 and Fig. 5). Extinction angle seems to increase abruptly thus ordering the control to increase firing delay (due to minimum extinction angle control) and increase the DC voltage on inverter side (Fig. 6).

This reduces the current on the inverter as well as rectifier terminals below the reference causing a decrease in rectifier firing delay (Fig. 5) and a subsequent sharp rise in rectifier voltage (Fig. 4) and rectifier current (Fig. 2). The problem is compounded when the current order increases from its fault-time value to rated value under the control of Voltage Dependant Current Order Limit (VDCOL) control, as shown in Fig. 2. The current which should initially have risen to fault-time limit (0.55 pu in this particular case), would now be commanded to rise to the normal operating condition.

As a result, the inverter current increases at a high rate (Fig. 1), much too high to increase the overlap duration to a level where available extinction time is not sufficient for
deionization and hence the commutation failures occur once again. Afterwards, the system makes another self-correcting attempt to recover to steady-state. A recovery to 90% of rated value for both inverter and rectifier currents is obtained somewhere after 1.5 s. This makes the recovery time more than 400 ms after the clearance of the original fault.

III. IN-DEPTH ANALYSIS

A comparison of inverter \( \alpha \)-order in Fig. 5 and inverter DC voltage in Fig. 3 reveals that the inverter DC voltage is rising sharply in the interval between 1.1 s and 1.2 s whereas inverter \( \alpha \)-order is not (there is however small variation with high frequency in inverter \( \alpha \)-order). A similar comparison between rectifier \( \alpha \)-order in Fig. 5 and rectifier DC voltage in Fig. 4 shows coherence between the two.

To elaborate on this, Fig. 7 shows the rectifier \( \alpha \)-order and \( \alpha \) measured from the two valve groups. There is an error between the reference and the actual values. This, however, is small and the actual values follow the command in general.

Fig. 8 shows ordered and measured \( \alpha \) values for inverter terminal. In the period of interest (i.e. after clearance of fault at 1.1 s), it is observed that the error between measured and ordered values is very high. This is the primary reason for steep rise in inverter voltage contrary to what is ordered by the minimum extinction angle control loop on the inverter side. A comparison with Fig. 7 shows that the measured and ordered \( \alpha \) in the case of rectifier side are very close by indicating good control.

The phase locked loops (PLL) embedded in the valve group control for this model have proportional gains equal to 10 and integral gains equal to 50 on both rectifier and inverter side. The time constant is therefore 0.2 s (10/50) which is quite large as it would take almost 5 time constants to reduce the error to a negligible level. This means that it will take much too long to eliminate the error between the reference and actual values at the inputs and outputs of these PLLs in comparison with the dynamic requirements of the system under consideration.

The question arises, why then the rectifier terminal is able to follow the \( \alpha \) order in contrast to the inverter terminal? The answer lies in the control loops involved in rectifier and inverter. The rectifier \( \alpha \)-order control loop extracts its reference from current order which is in turn generated by inverter DC voltage and DC current. The actual DC current at the rectifier is subtracted from this reference to generate the error. All of these are analogue signals in their nature and also pass through sensors with low-pass filtering characteristics. Hence, there is not a lot of high frequency component in these values. The \( \alpha \)-order for rectifier, therefore, does not contain much high-frequency component. A sketch of these details is shown in Fig. 9.

On the other hand, minimum extinction-angle control loop on the inverter side takes the measurement of extinction angle without any filtering. To complicate the matter further, this signal is fed to a “Minimum-in-one-cycle” module which updates its value after each power cycle. A conceptual sketch of this scheme is shown in Fig. 10. The output, thus, consists of steps with high frequency component as shown in Fig. 6. This signal is subtracted from reference minimum to generate
the \( \alpha \)-order for inverter. This signal would obviously contain high-frequency components as can be seen in Fig. 8. 

The PLL closed loop transfer function \( T_{PLL}(s) \) (ignoring all other dynamics in the system) in zero-pole-gain format, based on given values of proportional gain equal to 10 and integral gain equal to 50, is given by:

\[
T_{PLL}(s) = \frac{0.9091(s + 5)}{(s + 4.545)}
\]

(1)

Clearly, this transfer function does not have the adequate filtering characteristics for high frequencies. The higher frequencies in inverter \( \alpha \)-order thus pass through, destabilizing the output. On the other hand, these higher frequencies are not present in any signal in the control loop involving rectifier current controls, so the rectifier \( \alpha \)-order is successfully tracked by the actual values.

Another perspective is the time-domain view. The unit-step response \( a(t) \) for the transfer function given in (1) is:

\[
a(t) = 1 - 0.909e^{-t/0.22}
\]

(2)

The initial error is thus 0.0909 which would decay to zero in almost 1.1 s (5×0.22). So the property of PI control to eliminate steady-state error is not useful with these gain values and the dynamic requirements of the system being considered.

IV. SUGGESTED CHANGES AND SIMULATION RESULTS

The closed-loop transfer function for the PLL control block with unity feedback, arbitrary proportional gain \( K_P \) and integral gain \( K_I \) is given by (All other dynamics have been ignored in the loop):

\[
T_{PLL}(s) = \frac{1}{K_P + 1} \left[ \frac{sK_P + K_I}{s + \frac{K_I}{K_P + 1}} \right]
\]

(3)

The unit step response \( a(t) \) is the given by:

\[
a(t) = 1 - \frac{1}{K_P + 1} \left( \frac{s}{s + \frac{K_I}{K_P + 1}} \right)
\]

(4)

Equation (4) can be verified by putting the set values of proportional and integral gains in it. The results will be similar to (2). There are certain observations that need to be mentioned regarding (4). An intuitive thought would be to increase \( K_P \) to reduce the time constant for removing the error quickly. However, this does not have any effect on the initial value of the error which is dependant solely on \( K_P \). An increase in \( K_P \) would reduce the initial error which is desired but also increase the time constant for error elimination which, in the present context, may not be a strict requirement. The initial error with \( K_P \) equal to 10 is almost 9.09% whereas it would be 0.99% for \( K_P \) equal to 100. This would increase the time-constant to 2.02 s, but this is rendered insignificant due to the fact that the response would already be in a very close range instantaneously.

Using the above mentioned justification, simulations of the same HVDC system have been carried out, based on this value of \( K_P \) equal to 100 and \( K_I \) equal to 50. The time-domain plots for Inverter DC current is shown in Fig. 11, rectifier DC current and current-order are shown in Fig. 12, inverter DC voltage in Fig. 13, and rectifier DC voltage in Fig. 14. As is evident, there is no oscillation in currents and voltages after the clearance of fault at 1.1 s. The variables recover smoothly to almost 90% of rated values around 1.3 s, the recovery time being 200 ms. This is equivalent to an improvement of almost 50% on the basis of 400 ms recovery time observed in the original case.

To analyze what has improved in the system, refer to Fig. 15 showing \( \alpha \)-order for inverter and rectifier terminals, Fig. 16 outlining inverter \( \gamma \), Fig. 17 giving the account of \( \alpha \)-order and actual \( \alpha \) for rectifier terminal, and Fig. 18 showing \( \alpha \)-order and actual \( \alpha \) for inverter terminal.

As is obvious, the rectifier \( \alpha \)-order of Fig. 15 does not exhibit oscillations as compared to the one in previous case (Fig. 5). Inverter \( \gamma \) shown in Fig. 16 is also non-oscillatory. As discussed earlier, this plot would be composed of steps due to nature of control blocks that are employed in the model. Inverter \( \gamma \) is zero during fault period and after clearance of fault, it initially attains a high value due to smaller \( \alpha \)-order and actual \( \alpha \) at the inverter terminal. Minimum-extinction angle control mechanism slowly reduces this to the steady-state minimum meaning the restoration of inverter DC voltage as shown in Fig. 13. The rectifier \( \alpha \)-order and measured \( \alpha \) for both valve groups are coherent for the suggested scheme as shown in Fig. 17. This is similar to the behaviour exhibited by the original system as mentioned above and shown in Fig. 7. The only difference being no oscillations during post-fault period. Another thing worth noting is that the rate of change of \( \alpha \) for rectifier terminal is not very high which is due to the fact that the current order is not rising steeply as could be seen in Fig. 12. This absence of oscillations is attributed to the \( \alpha \)-order and measured \( \alpha \) for inverter shown in Fig. 18. In a strikingly contrasting manner to the plots for the same variables in Fig. 8, the actual values in Fig. 18 track the reference with very small error in the case with suggested modifications. This means that the voltage at
inverter terminal does not rise steeply, as shown in Fig. 13 (compare with Fig. 3). As this voltage is controlling the current order to the rectifier, there are no oscillations in the current order in this case as can be seen in Fig. 12 (compare with Fig. 2).

As the current order does not rise before it has to, the rectifier \( \alpha \)-order and voltage do not vary with high rate of change (Compare Fig. 15 and Fig. 14 with Fig. 7 and Fig. 4).

So the rate of change of rectifier and more critically inverter current is manageable with suitable extinction angle available as can be seen in Fig. 16. In contrast, extinction angle for original system would fall to zero between 1.16 s and 1.2 s indicating commutation failures as can be seen in Fig. 6.

In-short the suggested modification has changed the behaviour of the system from incomprehensible to exactly according to expectations.
V. CONCLUSION

Ride-through capability of first CIGRE benchmark for HVDC is tested by simulating fault at the inverter bus on the system modelled as an example case in PSCAD®/EMTDC. The post-fault behaviour of the link is analyzed in detail and reasons for control instability leading to post-fault commutation failures are investigated and exposed. A modification in the PLL driving the valve-groups at inverter terminal is suggested. Simulations have been carried out based on the suggested modification and the results are presented and evaluated. It is argued that the suggested control has reduced the recovery time by approximately half. The system under test is a weak system with both, rectifier and inverter SCR equal to 2.5. An investigation needs to be done whether the suggested scheme would yield improvements in even weaker systems or stronger systems. Preliminary work has been done in this regard and would be the topic of a future publication.

For the interest of the reader, a stronger system with an SCR equal to 10, with original control parameters does not experience any post-fault commutation failure, and on the other hand, a weaker system with an SCR equal to 1 is unstable without any faults.

REFERENCES