Effects and Mitigation of Post-Fault Commutation Failures in Line-Commutated HVDC Transmission System

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Abstract—This work analyzes post-fault commutation failures and their effects in a thyristor based line commutated HVDC link. Simulation results of the example case available in PSCAD® reveal these failures. Two schemes have been suggested to mitigate these effects. Simulations of the suggested schemes show that these can swiftly and effectively control fault currents as well as post fault commutation failures.

Index Terms—HVDC Transmission, Power Electronics, Thyristor Converters

I. INTRODUCTION

HVDC is the preferred way of controlling power flow over large distances and these distances become very short where underground or submarine power transmission is considered. Interconnection of asynchronous systems with different control philosophies and different frequencies are also the applications where HVDC becomes inevitable [1].

There are two topologies for HVDC transmission namely Current Source Converter (CSC) [1] and Voltage Source Converter (VSC) [2], former being the older of the two. In CSC transmission, the magnitude and direction of flow of DC current is kept constant while the line voltage polarity is reversed for power flow reversal. On the other hand, in VSC transmission, the DC line voltage is held constant while the current flow is reversed for reversal of power flow.

CSCs, also referred to as Line Commutated Converters (LCC), involve ac to dc conversion via natural commutation of current from one thyristor in a bridge to the other one. The only control being that of firing instant at which a thyristor should start conducting from the time it is capable of conducting. Once a thyristor starts conducting it will continue to conduct till the time the next thyristor in the bridge is fired with the commutation voltage favoring it and the current commutating naturally from the outgoing thyristor to the incoming thyristor. This makes the CSC technology slow as well as a sink of reactive power as the line current will always lag the phase voltage [1].

VSCs, also referred to as the Forced Commutated Converters, involve fast controllable switches which can start and stop conduction of current at the “will” of the control. The switching frequency of valve arms in such devices is quite high when compared to the power frequency [2]. VSCs can act as reactive power sources, a big plus besides others for this type of converters over the conventional CSC technology. However, dynamic balancing of voltage appearing across individual modules in a valve upon forced switch-off is still a problem raising questions about reliability of such converters for very high power rating [2].

Nevertheless, CSC technology is considered a much more mature technology and it continues to develop with increasing interest in HVDC transmission as energy demands grow. There are continuous improvements being carried out in the control and design of CSCs to conceive and cater for as many contingencies as possible.

One of the problems that are encountered during the operation of a power system is the occurrence of a short circuit in the transmission system. To maintain the system in proper working condition, controls have been introduced and developed to keep the converter stations in working order and recover to normal operation upon fault clearance. However, problems are encountered during recovery from a fault as mentioned in [1] and [3] but have not been discussed in detail. Another perspective on the problem is provided in [4].

This work is related to the study of this problem and suggests measures to limit the same. The CIGRE benchmark for HVDC [5] has been chosen for simulation purposes as it is already implemented in PSCAD® / EMTDC as an example case. The reason for the selection of this model is the presence of numerous system difficulties that may be encountered in a real system which have been explained in [5].

II. SIMULATIONS

The schematic of the model used for simulation is shown in Fig. 1 with some important parameters mentioned in Table I. The model under test is a single pole HVDC Link with major parameters set out in Table I. For details, the reader is referred to [5]. Focus of this work is the modification in the control of the system to eliminate commutation failures which are observable in the available model. Three cases have been
simulated, the first one giving an insight into the problems in the existing model, while the other two representing the results obtained by applying two different approaches to mitigate the problem in question.

For all cases, the simulations have been done from a snapshot file which was created by running the system simulation without any fault for 5 seconds and with a simulation step size of 10 μs. Thereafter, fault simulation with a 3-phase-to-ground fault of 10 ms duration occurring at 0.1 ms on the inverter ac bus has been carried out. The observed parameters are the inverter and rectifier side currents as well as the voltage dependant current order limit (VDCOL) and current and angle orders for rectifier.

A. Case I

The results of the simulations are presented in Fig. 2 to Fig. 6. It is evident that after the clearance of fault at 0.2 s, there are current spikes at both the rectifier and inverter DC bus which are almost equal in magnitude to the initial fault current levels. Consequently, normal operation is resumed at around 0.4 s which is almost 200 ms after the clearance of the fault.

Current order to the rectifier is generated by selecting the minimum from the settable current order (which in this case is 1 PU) and the output of voltage dependant current order limit (VDCOL) function. This scheme is depicted in Fig. 7. VDCOL has been implemented using a transfer function whose minimum value is maintained at 0.55 for all inputs below 0.4. For inputs ranging between 0.4 and 0.9, the output of the function increases/decreases linearly between 0.55 and 0.9. Beyond the upper input threshold of 0.9, the gain of this function is unity. A graphical interpretation of this implementation is shown in Fig. 8. Fig. 4 depicts the output of this function for the simulation under discussion. The current order to the rectifier as shown in Fig. 5 is a replica of the voltage dependant current order limit except that it does not exceed the maximum value of 1 PU due to the reason explained earlier. Control of angle order for rectifier is based on the rectifier current order, the reason why it is following the pattern as observed in Fig. 6 i.e. firing angle is small for higher current order and vice versa.

The facts mentioned above make it easier to understand that there is no damping provided for the rise in current order for rectifier thus instantaneously reducing the firing angle without the voltage having risen to the proper level for proper operation. This causes commutation failures and the delay in the restoration process. Due to commutation failures, the DC link voltage again goes down causing an abrupt decrease in the

### TABLE I

<table>
<thead>
<tr>
<th>S. No.</th>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>Rated DC Link Voltage</td>
<td>500</td>
<td>kV</td>
</tr>
<tr>
<td>2.</td>
<td>Rated Power</td>
<td>1000</td>
<td>MW</td>
</tr>
<tr>
<td>3.</td>
<td>AC System Frequency</td>
<td>50</td>
<td>Hz</td>
</tr>
<tr>
<td>4.</td>
<td>Rectifier SCR</td>
<td>2.5 @ 84°</td>
<td></td>
</tr>
<tr>
<td>5.</td>
<td>Inverter SCR</td>
<td>2.5 @ 75°</td>
<td></td>
</tr>
<tr>
<td>6.</td>
<td>Rectifier Side AC Voltage (L-L RMS)</td>
<td>345</td>
<td>kV</td>
</tr>
<tr>
<td>7.</td>
<td>Inverter Side AC Voltage (L-L RMS)</td>
<td>230</td>
<td>kV</td>
</tr>
</tbody>
</table>
current order triggering an abrupt firing angle advance which is the cause of the dip in inverter and rectifier currents. Afterwards, the system slowly settles down to the set-point values.

B. Case II

As discussed, there is a need to add damping in the current order control path so as to increase the rise time and control the oscillations encountered in case I. This has been done by adding a first-order pole in the control loop, as shown in Fig. 9. The gain G of the pole is unity, whereas the decay time constant T for this pole has been set at 0.05 s. The location of this pole is between the input to the rectifier angle order reference and the output of the minimum selected from set value of current and VDCOL.

The effects of addition of this pole are shown in Fig. 10 to Fig. 14. It is evident (from Fig. 10 and Fig. 11) that the post-fault current spikes observed in case I (Fig. 2 and Fig. 3) have been eliminated by the addition of this control function. Both the inverter and rectifier currents return to satisfactory levels at approximately 0.3 s i.e. 100 ms after the clearance of the fault. This is half the time required for recovery in case I.

The reason for this action becomes clear from inspection of Fig. 12, Fig. 13 and Fig. 14. The Output of VDCOL (Fig. 12) and current order to rectifier (Fig. 13) are not identical, contrary to what had been observed in case I (Fig. 4 and Fig. 5). The pole introduced, modifies and damps the current order to the rectifier producing a corresponding damping in the angle order to the rectifier bridges (Fig. 14). Therefore, the angle order in case II does not possess the post-fault oscillations as observed in case I (Fig. 6).

However, a close inspection of Fig. 13 reveals that due to the introduced damping in the current order path, the current order falls slowly in case II if compared to case I (Fig. 5) at the time of initiation of fault. This slows down the increase in the firing angle and actually limits it to a lower value as shown in Fig. 14 as compared to Fig. 6. Due to this, fault current magnitudes in Fig. 11 and Fig. 12 are comparatively higher than those in Fig. 2 and Fig. 3, respectively.

Therefore, there should be a mechanism which should not damp out the firing angle advance during fault to limit the fault.
current and which should also damp out the pull back of firing angle order in order to avoid post-fault commutation failures.

C. Case III

In order to eliminate the problem discussed above in case II, a bypass mechanism for the introduced damping is required during the fault to limit the fault current.

This has been achieved by changing the location of the first-order pole from the position in case II. The new position is obtained by a careful analysis of Fig. 12 and Fig. 13. If the dropping characteristic of VDCOL is selected and rising characteristic of the first-order pole is selected to formulate the current order for the rectifier, it would serve the purpose of rapid advance of firing order during fault and damped recovery during post-fault period.

This has been achieved by first placing the first-order pole after VDCOL. Then the minimum among the unfiltered VDCOL, filtered VDCOL, and settable current order is selected to generate the current order and in turn the firing angle order for the rectifier. Fig. 15 represents the implementation explained above.

The effects of this scheme are shown in Fig. 16 to Fig. 20. It is observed in Fig. 16 and Fig. 17 that the post-fault behavior is almost identical to Fig. 10 and Fig. 11 i.e. the currents recover to the set values in approximately 100 ms without any spikes.

The fault current peaks in case III are dissimilar to those observed in case II and are like those of case I. This means that effective control over fault current magnitudes has been achieved by the technique employed here compared to case II.

The reason for this control becomes evident from an analysis and comparison of VDCOL, current order and angle order for case III (Fig. 18 to Fig. 20) with those of case II (Fig. 12 to Fig. 14) and case I (Fig. 4 to Fig. 6). The current order shown in Fig. 19 drops instantaneously just like the one in Fig. 5 and in contrast to the one shown in Fig. 13 during fault. On the other hand, after fault clearance, the current order of case III rises in a damped manner like case II and not like case I.

That is why angle order for rectifier shown in Fig. 20 behaves in a similar fashion to the one shown in Fig. 6 at the time of inception of fault as opposed to the one shown in Fig. 14. The maximum value of angle order in case III is approximately the same as that of case I, the reason for effective fault current control. On the other hand, the angle order in case III behaves similarly to the one for case II after fault clearance and not like the one in case I.

Therefore, fault current reduction capability of case I and post fault commutation failure mitigation capability of case II have been combined in case III.

III. CONCLUSION

The problem of post-fault commutation failure in thyristor based line commutated HVDC link with regards to current patterns observed at the inverter and rectifier buses has been analyzed. The current patterns observed have been explained.
by analyzing the underlying current control mechanisms. The deficiencies in the control system have been identified.

Based on the deficiencies identified in the control mechanism for current, a scheme has been devised to mitigate the post-fault commutation failures. A comparison of the simulation results obtained from the employed scheme with those of the original model show promising results as far as the post-fault commutation failures and current magnitudes are concerned. These have been explained by observing different signals involved in firing angle control of rectifier side.

However, further investigation reveals that the scheme employed to mitigate post-fault problems slows down the fault-current control of the system as well. Based on this observation, a second scheme has been suggested which does not disturb the control mechanism of the original system during fault and damps the current order rise after fault to mitigate post-fault problems. The simulation results for this scheme show effective control over fault current magnitudes as well as post-fault commutation problems.

During all of this, the firing angle control of the inverter side, responsible for voltage adjustment on the link, has not been considered. Though, the current control of rectifier side indirectly influences the firing of the inverter bridges as well, it has been ignored. An investigation may be carried out to determine the effect of inverter voltage control mechanism on fault and post-fault problems discussed here. We have observed that there is essentially no difference in the angle order for inverter in all the three cases.

An empirical value for the time constant of the first-order pole used in the suggested scheme has been used. An optimum value for this time constant to cover all types of commonly occurring faults and for most common fault durations needs to be investigated.

The suggested schemes could also be tested for different fault types with different fault durations, and different locations (i.e. on the rectifier bus with varying strengths on rectifier and inverter side AC systems).

REFERENCES