Abstract—The paper focuses on a method to interface a power buffer based on supercapacitors (SCs) to a system with a stiff DC voltage. An optimized design methodology is given, showing that the proposed system is able to fully control the power flow between the SCs and the DC-link, making use of reduced-rating switching devices and magnetic components. Losses of the proposed system are analytically evaluated and compared to those of a standard Half Bridge interface. A prototype of the converter to be used on board of an existing city-vehicle is built. The vehicle is equipped with a 240V battery and an inverter/motor system with a peak power of 30 kW. Experimental results on such a real-scale prototype validate the theory and show the feasibility of the proposed approach.

Keywords — Hybrid source, DC-DC converter, EDLC, Supercapacitor, Energy Management.

I. INTRODUCTION

Electric Double Layer Capacitors (EDLC), also known as supercapacitors (SC), are gaining popularity as secondary sources of power in applications where relatively short bursts of power have to be supplied to the load, relieving the stress on the primary energy source [1-3], with the result of extending the lifetime of the system and increasing the overall efficiency. In automotive systems, the primary source can be either a battery with relatively high energy density, or a fuel cell; the most widespread kind of load is an AC motor, fed through an inverter. In such systems, the power buffer constituted by the bank of SCs is interfaced to a relatively stiff DC voltage. Parallel connection without Power Electronics interface is an option, having the obvious advantage of simplicity; however, the power flow between the two sources and the load cannot be explicitly controlled and, perhaps more important, only a very small part of the energy available in the SC buffer can be used by the load, due to the voltage constraint of the stiff DC voltage. In fact, SCs are capacitive in nature, meaning that their terminal voltage is strongly dependent on their energy content, or state of charge (SOC). In other words, we must be able to operate the SC bank at variable terminal voltage, if we want to charge/discharge the power buffer. Several kinds of power electronics converters exist, that are suitable for the task. In [4], different topologies are reviewed and compared, and the simple Half-Bridge (HB, shown in Fig.1-a) is found as the best option. As a matter of fact, in virtually all implementations of hybrid Battery-SC and in the majority of FC-SC energy sources found in the literature, the SC power buffer is interfaced to a DC link by a bidirectional HB converter [4-7]. In some works [8, 9], the HB topology has been split into several legs, controlled with an interleaved PWM pattern; main advantage of this technique is the volume reduction of the bulky inductor, but the total Volt-Ampere rating of the semiconductors is not reduced, compared to the base case of single leg HB. In [10, 11], the assumption of stiff DC voltage at the output terminals of the SC power buffer is used to develop a new topology using smaller power electronics switches (about half the Volt-Ampere ratings of what would be required by an equivalent HB) and much smaller magnetic components.

In this paper, an analytical method for optimized design of such a reduced VA converter is given, taking into account not only the maximization of the useful energy in the power buffer, but also the overall system efficiency and the distribution of losses. Then, experiments on a full-scale prototype of the proposed converter, designed to work on a small electric vehicle and capable of delivering 30kW of power for more than 15 seconds, are presented to validate the analysis.

II. OPERATING PRINCIPLE OF THE PROPOSED CONVERTER

The proposed system (Fig.1-b), referred to as HC (Half Controlled) converter system in the following, makes use of a series connection of two SC banks and two power electronics switches connected across one of them. Due to the series connection, it is easy to recognize that SC0 is charging/discharging with the current \( I_{\text{SC0}} \), that is the load-side current of the power buffer. Charge/discharge of the bank SC1 is controlled by the state of the switches, which are also used to control the current \( I_{\text{SC1}} \) as required by the load. It is shown in [10] that in the ideal, lossless system of Fig.1-b, the terminal voltages of the two SC banks are always related by:

\[
V_{\text{SC1}}(t) = \sqrt{V_{\text{SC0}}(0)^2 + C_{\text{SC0}} \frac{d}{dt} \left( 2(V_{\text{DC}} - V_{\text{SC0}}(0)) \Delta V_{\text{SC0}}(t) - \Delta V_{\text{SC0}}(t)^2 \right)} (1)
\]

with: \( \Delta V_{\text{SC0}} = V_{\text{SC0}}(t) - V_{\text{SC0}}(0) \)

The key equation above allows us to design the two SC banks so that they charge and discharge evenly, regardless of the particular time trajectory of the converter output current. In particular, assuming as initial condition both

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SC banks fully charged to their rated voltage ("buffer full" state), the capacitance ratio:

\[ x = \frac{C_{SC,0}}{C_{SC,1}} \]  

(2)

can be used to maximize the amount of energy that can be extracted from the SC banks before the bottom equilibrium condition is reached. Such a condition is defined by the voltage balance:

\[ V_{DC} = V_{SC,0} + V_{SC,1} \]  

(3)

when the converter is no longer able to control the load current; we refer to this condition as the "buffer empty" state. The fraction of the total energy content of the SC banks that can be used by the load as a function of the design parameter \( x \) defined by (2) is plotted in Fig. 2-a.

Since the system is assumed to be lossless, the SC banks will ideally cycle between the "buffer full" and "buffer empty" states, as current is cycled in and out the SC buffer.

III. DESIGN CRITERIA FOR THE OPTIMUM CAPACITANCE RATIO, TAKING LOSSES INTO ACCOUNT

If the only criterion for system design is the maximization of the amount of energy that can be extracted from SC banks, then the solution is uniquely determined by Fig. 2-a: \( x = 2 \) maximizes the amount of usable energy in the power buffer, as it was shown in [11]. However, it is also important to find out how the capacitance ratio influences the total losses and their distribution within the system. Moreover, it is meaningful to compare the amount of losses expected while cycling energy in and out the SC buffer using the proposed topology of Fig. 1-b, with the losses of an equivalent system based on the conventional HB topology of Fig. 1-a.

In this context, the two systems in Fig.1 are said to be equivalent if the following conditions are met:

1. They are connected to the same DC link:
   \[ V_{DC,HB} = V_{DC,HC} = V_{DC} \]

2. They are able to exchange power with the load at the same maximum rate \( P_{out,max} \), throughout the whole charge/discharge process. In short:
   \[ P_{out,max} = V_{DC} \cdot I_{HB,max} = V_{DC} \cdot I_{HC,max} \]

3. They have the same energy storage capability in the respective SC buffer, and they are able to utilize at least 75% of such total energy, while being charged/discharged at rated power.

4. SC banks in both systems are optimized in voltage; that means:
   \[ V_{SC,HB,max} = V_{DC}, \text{ and } V_{SC,0,max} = V_{SC,1,max} = V_{DC} \cdot x \]

In the HB converter system there is only one SC bank; its maximum energy content is related to the rated terminal voltage and the bank capacitance by:

\[ E_{SC,max} = \frac{1}{2} C_{SC,HB} \cdot V_{SC,max}^2 = \frac{1}{2} C_{SC,HB} \cdot V_{DC}^2 \]  

(4)

In the HC converter system there are two SC banks; the total maximum energy is the sum of the individual energies:

\[ E_{SC,max} = \frac{1}{2} (C_{SC,0} \cdot V_{SC,0,max}^2 + C_{SC,1} \cdot V_{SC,1,max}^2) \]

\[ = \frac{1}{2} (C_{SC,0} + C_{SC,1}) \cdot V_{DC}^2 \]  

(5)

In order to have the same energy content in the two systems (condition 3. for equivalence) it must therefore be:

\[ C_{SC,HB} = C_{SC,0} + C_{SC,1} \]  

(6)

Applying the definition of capacitance ratio \( x \), as defined by (2), we get:

\[ C_{SC,HB} = \frac{x+1}{x} \cdot C_{SC,0}, \quad C_{SC,1} = \frac{x}{x+1} \cdot C_{SC,HB} \]  

(7)

It follows that once we have fixed a given amount of total energy, determined by the load cycle requirements, the capacitance needed in the HB system is uniquely determined by (4), while the capacitances of the two banks in the equivalent HC system are function of the capacitance ratio, as stated by (7).

A. Losses in the supercapacitors

Supercapacitors are not ideal. They have an equivalent series resistance (ESR) that gives rise to losses when current is flowing to charge/discharge the power buffer. In general, the amount of losses is dependent on the particular trajectory of the converter output current during

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**Figure 1.** Different topologies for power flow control of SC-based power buffer interfaced to a DC link.
the cycle; in the following, a complete discharge at constant current is used as benchmark. Though simple, the cycle is significant since it gives a close-to-worst case scenario if the constant current is fixed at the rated value; the choice of a simple current trajectory also allows us to find analytical solutions that are parametric in \(x\), which is the main design parameter. A further simplification in the analytical calculation of losses is the assumption of ideal components to determine the voltage and current waveforms; the idealized waveforms are then used to evaluate losses in non-ideal components.

For the HB topology, the amount of energy dissipated in the ESR of the SC bank during a complete discharge from rated SC voltage to half of it (corresponding to 75% energy extraction) is given by:

\[
E_{SC,HB} = \int_{0}^{\frac{1}{2}T_{dis}} I_{SC,HB}^2(t) \cdot ESR_{SC,HB} \cdot dt
\]

\[
= I_{dis} \cdot ESR_{SC,HB} \cdot \frac{T_{dis}}{1.85}
\]

(8)

In the equation above, \(T_{dis}\) is the time needed to discharge 75% of the total energy content of the SC buffer at a constant power rate \(P_{out} = V_{DC} \cdot I_{dis}\).

In the HC topology there are two SC banks; their capacitance is related to the capacitance of the equivalent HB system by (7). With the assumption of constant Ohm-Farad product, ESR of each bank will be related to the ESR of the single bank in the equivalent HB system by:

\[
ESR_{SC,0} = ESR_{SC,HB} \cdot \frac{x+1}{x}
\]

\[
ESR_{SC,1} = ESR_{SC,HB} \cdot (x+1)
\]

(9)

HC system discharge losses are then:

\[
E_{SC,HC} = E_{SC,0} + E_{SC,1}
\]

\[
= ESR_{SC,0} \int_{0}^{\frac{1}{2}T_{dis}} I_{SC,0}^2(t) \cdot dt + ESR_{SC,1} \int_{0}^{\frac{1}{2}T_{dis}} I_{SC,1}^2(t) \cdot dt
\]

\[
= ESR_{SC,HB} \frac{x+1}{x} \int_{0}^{\frac{1}{2}T_{dis}} I_{SC,0}^2(t) \cdot dt + ESR_{SC,HB} (x+1) \int_{0}^{\frac{1}{2}T_{dis}} I_{SC,1}^2(t) \cdot dt
\]

(10)

The ratio between the total losses in the SC banks of the two systems is shown in Fig. 2-b. It can be seen that SC losses are always slightly higher in the HC, as compared to HB, for any possible capacitance ratio of the former. However, the difference is below 10% for a wide range of \(x\) between 2.1 and 3, with a minimum of 8.3% for a capacitance ratio \(x = 2.56\).

In HB there is only one SC bank, and therefore all the nominally identical SC cells constituting the bank are equally stressed; on the other hand, in HC there are two banks and each of them is subject to a different current flow during cycling. It is then important to understand how losses are distributed among the two banks. Total losses are given by (10), where individual contribution of each SC bank is also visible. For the individual SC cells to be equally stressed, losses among the two banks should be distributed according to their capacitance ratio (the biggest bank should bear the biggest share of losses). We can then define the normalized loss ratio as:

\[
\rho_{HC} = \frac{E_{SC,0}}{E_{SC,1}} = \frac{I_{dis}^2 \cdot T_{dis}}{x} \cdot \left( \int_{0}^{T_{dis}} I_{SC,1}^2(t) \cdot dt \right)^{-1}
\]

(11)

Such a function is reported in Fig. 2-c. It can be observed that for a capacitance ratio of 2.4, the two SC banks are equally stressed, under the assumption of constant Ohm-Farad product. The bigger SC bank (SC0) is more stressed for lower capacitance ratios, while the opposite happens for higher \(x\).

Combining the information contained in the three plots of Fig. 2, we have a good insight for optimum design of the SC banks in the HC system of Fig. 1-b. As a guideline, the capacitance ratio should be designed to have a value between 2 and 3. In fact, if the ratio is bigger than 3, energy utilization tends to become poor (less than 75%); on the other hand, a ratio lower than 2 leads to increased (and unbalanced) losses in the SC banks. Since both the energy extraction curve and the figure of total losses are quite flat around those reasonable capacitance ratios, the actual choice of \(x\) can be determined by the availability of actual SC cells used to build up the two banks. An example is given in the following, when presenting the experimental setup.

B. Losses in the semiconductor switches

Semiconductor devices used to implement the converter switches have both conduction and switching losses. In order to simplify the calculations, we will assume that active switches and anti-parallel diodes have the same conduction characteristics. Moreover, we will assume that the voltage drop across the conducting device can be approximated as the sum of a constant voltage drop plus a resistive drop:

\[
V_f = V_{f,0} + R_f I
\]

(12)

This approximation applies quite well to bipolar devices like IGBTs and power diodes.

1) HB topology – Conduction losses

Whatever the status of the switches, the SC-side current...
is flowing either into one switch (the lower, during SC discharge) or one diode (the upper, during SC discharge).

\[
E_{S,\text{cond},HB} = \int_0^{T_{\text{dis}}} V_{f,0} \cdot I_{SC} \cdot dt = \int_0^{T_{\text{dis}}} (V_{f,0} + R_f I_{SC}) \cdot I_{SC}^2 \cdot dt
\]

\[
= V_{f,0} \cdot \int_0^{T_{\text{dis}}} I_{SC} \cdot dt + R_f \cdot \int_0^{T_{\text{dis}}} I_{SC}^2 \cdot dt
\]

\[
= \frac{4}{3} \cdot V_{f,0} \cdot I_{\text{dis}} \cdot T_{\text{dis}} + 1.85 \cdot R_f \cdot I_{\text{dis}}^2 \cdot T_{\text{dis}}
\]

(13)

2) HB topology – Switching losses

Switching losses in the high-side switch are negligible during SC discharge (current is in the diode, and we neglect reverse recovery losses). Instead, there will be both turn-on and turn-off losses in the low-side switch (the situation is reversed during SC charging):

\[
E_{S,\text{sw},HB} = \int_0^{T_{\text{dis}}} (dE_{\text{on}} (I_{SC}, V_{DC}) + dE_{\text{off}} (I_{SC}, V_{DC})) \cdot f
\]

\[
= \int_0^{T_{\text{dis}}} \left( I_{SC} \cdot V_{DC} \cdot (E_{\text{on}} (I_n, V_n) + E_{\text{off}} (I_n, V_n)) \right) \cdot dt \cdot f
\]

\[
= T_{\text{dis}} \cdot \frac{4}{3} \cdot V_{DC} \cdot I_{\text{dis}} \cdot \left( E_{\text{on}} (I_n, V_n) + E_{\text{off}} (I_n, V_n) \right) \cdot f
\]

(14)

having made the simplifying assumption of losses increasing linearly with current and voltage. Instead, the figures of elementary turn-on/turn-off losses at rated current and voltage \(E_{\text{on}}, E_{\text{off}}\) are normally available in the component datasheets.

3) HC topology – Conduction losses

Similarly to the HB case, there will always be either one switch or one diode on the current path.

\[
E_{S,\text{cond},HC} = \int_0^{T_{\text{dis}}} (V_{f,0} + R_f I_{\text{dis}}) I_{\text{dis}} \cdot dt
\]

\[
= V_{f,0} I_{\text{dis}} \cdot T_{\text{dis}} + R_f I_{\text{dis}}^2 \cdot T_{\text{dis}}
\]

(15)

Direct comparison of (13) with (15) is not possible unless some assumptions are made on the characteristics of the switch. To that purpose, let us assume that the switches are designed to have a forward voltage drop equal to 2.5 V at rated current, with a threshold voltage of 1.0 V. If the very same kind of switches is then used in HC, the ratio of conduction losses is:

\[
\frac{E_{S,\text{cond},HC}}{E_{S,\text{cond},HB}} \bigg|_{I_{\text{dis}}=I_{\text{dis}}=I_{\text{dis}}} = \frac{1.0 + 0.75}{4 \cdot 1.85 \cdot 0.75} = 0.64
\]

(16)

showing that conduction losses are greatly reduced in the HC system. Perhaps a more significant comparison is when the current rating of the switch used in HC is also optimized:

\[
\frac{E_{S,\text{cond},HC}}{E_{S,\text{cond},HB}} \bigg|_{I_{\text{dis}}=I_{\text{dis}}=I_{\text{dis}}} = \frac{1.0 + 1.5}{3 \cdot 1.85 \cdot 0.75} = 0.92
\]

(17)

This result is significant, since it shows that conduction losses in HC are smaller than those in HB, even if switches with half current rating (and therefore roughly double forward resistance) are used.

4) HC topology – Switching losses

\[
E_{S,\text{sw,HC}} = \int_0^{T_{\text{dis}}} (dE_{\text{on}} (I_{\text{dis}}, V_{SC1}) + dE_{\text{off}} (I_{\text{dis}}, V_{SC1})) \cdot f
\]

\[
= T_{\text{dis}} \cdot \frac{I_{\text{dis}}}{I_n} \cdot V_n \cdot (E_{\text{on}} (I_n, V_n) + E_{\text{off}} (I_n, V_n) \cdot f \int_0^{T_{\text{dis}}} V_{SC1} \cdot dt
\]

(18)

The integral in (18) can be solved analytically, though the solution is not reported here, since it is unnecessarily complex. It suffice to say that the result of the integration is almost independent of the capacitance ratio \(x\), and the total switching losses for HC are about 66% of the switching losses of HB, if the same device is used.

C. Considerations about losses in HC converter system

Looking at Fig. 2.b, one could conclude that the HC system is less efficient than an equivalent system based on HB. However, losses in Fig. 2.b are only the ones related to the ESR of the SC cells constituting the power buffer. Total system losses also include those generated in the power electronics switches, the smoothing inductor, and the electrolytic capacitors. It has already been shown that the losses in the semiconductor switches are reduced in the HC system; due to space limitations, a punctual analytical evaluation of losses in the other components is not reported here. However, it can be said that losses in most of the converter components are reduced in the HC system, and such a reduction more than offsets the increase of losses in the SC cells.

D. Downsizing of the DC inductor in HC converter system

Besides the reduction of losses in the power electronics converter components, perhaps the most remarkable advantage of HC is the downsizing of such components. In [10] it has already been shown that the necessary Volt-Ampere rating of the solid state switches of HC is about half of that of an equivalent HB; what was not pointed out is the possibility for considerable downsizing of the bulky inductor, due to the reduced peak current capability of the inductor used in the HC system, where only the load-side current flows in the inductor, regardless of the state of charge of the SC banks. In the HB system, the inductor has to carry the SC-side current, which can be as much as twice the load-side current, at the bottom of discharge.

As a practical example, we can consider the inductor shown in Fig. 3, designed for the HC converter system used in the experiments, rated at 30 kW continuous, with a DC-side voltage of 240 V. The full-load inductance is 0.15 mH, with a peak current of 140 A; resulting worst-case current ripple is about 30 A peak-to-peak, with a
switching frequency of 10 kHz. An amorphous core material is used, achieving a total weight of 3.0 kg. If the same worst-case ripple has to be achieved by an equivalent HB topology, the inductor should have 0.2 mH inductance, with a peak current capability of 265 A. Using the same core material, total weight is more than tripled, reaching 9.3 kg. Obviously, weight and ripple can be reduced by splitting the inductance and using interleaved PWM with multiple converter legs; however, such a technique can be applied to both HB and HC topologies and, for the sake of brevity, is not considered here.

IV. FULL-SCALE PROTOTYPE OF HC CONVERTER SYSTEM

In order to prove the feasibility of the proposal, a full scale prototype of the HC system shown in Fig. 1-b has been built. Specifications of the power buffer are given in Table I, and have been chosen according to the needs of an existing city-car (namely, the Norwegian Th!nk EV).

Each of the two SC banks is made up by series connecting 90 elementary cells, individually rated at 2.7 V, yielding a total bank voltage of 243 V. The bigger bank uses 1500 F cells, while the smaller uses 650 F cells, resulting in a capacitance ratio $x = 2.3$. According to Fig. 2, theoretical energy utilization is almost 77%; total SC losses are close to their minimum and are well distributed among the two banks. The two solid state switches are implemented with 600 V, 150 A IGBTs with related antiparallel diode. The layout of the system used in the experiments is given in Fig. 4. Due to the unavailability of the 240 V traction battery the power buffer was designed for, the DC-link is taken from the 220 V DC network of our lab facility. Moreover, there is no additional load, meaning that the power is transferred back and forth between the SC-based power buffer and the DC network. The HC system also features a low power dynamic balancing circuitry [12], whose purpose is to compensate for system losses, by forcing the system to track the ideal voltage trajectory defined by (1) [11]; rated current of the balancing bridge is 10 A, which is less than one tenth of the main HC current. Fig. 5 shows a picture of the prototype of the 30 kW, 240V, HC-based power buffer.

V. EXPERIMENTAL RESULTS

A. Charge/discharge cycle at low power

In the experiment of Fig. 6, the power buffer is cycled at low power. At first, the buffer is discharged with a constant current command of 31 A (25% of the rated current) down to the bottom limit defined by (3); it is possible to notice the natural decay of the converter current at the end of discharge when the voltage balance is approached and control is no longer possible. Then the buffer is charged with a constant current of the same magnitude until the top limit is reached; at this point, the bank SC0 reaches the DC-side voltage and no more energy can be pushed into the buffer, so that the converter output current naturally decays to zero. Throughout the whole charge/discharge process, the voltage profile follows the ideal trajectory defined by (1); this is true regardless of the particular waveform of the converter output current, as can be observed by the remaining part of the experiment, where an arbitrary load current is imposed. Since at such a low power rate the system losses are negligible, the ideal voltage trajectory is naturally followed, with almost no effort from the balancing circuitry.
circuitry, thus validating the theory.

B. Charge/discharge cycle at high power

Fig. 7 shows a charge/discharge process with a constant current of 100 A (80% of rated). In this case, losses cannot be neglected and the voltage trajectory deviates from (1); however, the action of the balancing circuit stabilizes the system. Under this heavy load condition, it is possible to evaluate the overall losses of the system by measuring the DC-side power over one complete charge/discharge cycle. By numerical integration of such a power and noticing that the energy stored into the SC buffer is the same at the beginning and at the end of each cycle, we calculated an average value for the losses of about 1.2 kW. Taking into account all the inaccuracies coming mainly from measurement offset and numerical integration, we can conclude that there is a good agreement between the theoretical losses summarized in Table II and the measured value.

VI. CONCLUSION AND FURTHER WORK

The advantages of a dedicated topology for power flow control between a power buffer based on supercapacitors and a primary energy source characterized by a constant terminal voltage have been clarified. The system is designed following a procedure ensuring good utilization of the energy available in the SC buffer, as well as high efficiency. Experiments on a real-scale prototype validate the theory, showing the feasibility of the approach.

REFERENCES


Figure 7. Experimental results; Cycles at constant output current (80% of rated), with calculation of cycle average losses.