An Optimized Converter for Battery-Supercapacitor Interface

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Abstract—A converter topology suitable for bidirectional power flow control between a supercapacitor bank and a stiff voltage source is presented. Main feature of the topology is the reduced ratings of the solid state devices used in the converter, as compared to conventional solutions. For the same capabilities in terms of energy extraction, reduction of up to 50% in the ratings of the silicon switching devices is achieved. Both simulations and experiments are performed to validate the principle.

I. INTRODUCTION

Electric Double Layer Capacitors, also known as Ultracapacitors or Supercapacitors (SC), are emerging as energy storage devices capable of delivering large amount of power over relatively short time; however, their low energy density makes them unsuitable for use as primary energy storage in most systems. Combined use of batteries and supercapacitors has proven very beneficial in applications with large peak-to-average power ratios, such as Electric Vehicle and traction systems [1-6]. The basic idea behind such a hybrid energy storage system is to use the relatively energy dense battery as source of the bulk energy, while the power dense supercapacitors provide (or absorb) the power peaks, as schematically shown in Fig.1.

The power electronics interface between the two sources has to allow for bidirectional power flow, and must be able to efficiently extract and push as much energy as possible into the costly supercapacitor buffer. Overall efficiency, EMI compliance, volume, reliability and cost also play a role in the selection of the most suitable interface. In [7], several bidirectional, hard-switched Power Electronics converter topologies have been analyzed and compared, concluding that the very simple half-bridge is to be preferred in most applications.

A. Operating Principle

In its basic configuration, the proposed system consists of the series connection of two banks of supercapacitors and a half bridge converter connected across one of the banks, as shown in Fig. 2.

In all operating conditions satisfying both (1) and (2), it is possible to control the current $I_{SC}$ acting on the duty cycle $D$ of the half bridge.

Due to the presence of the free-wheeling diodes, operating limits of the system are identified as follows:

$$V_{SC,1} + V_{SC,0} \geq V_{DC}$$

$$V_{SC,0} \leq V_{DC}$$

In all operating conditions satisfying both (1) and (2), it is possible to control the current $I_{SC}$ acting on the duty cycle $D$ of the half bridge.

Due to the series connection, current $I_{SC,0}$ flowing through the lower SC bank is always equal to the inductor current, while the current in the upper SC bank $I_{SC,1}$ is related to the inductor current by the bridge duty cycle (assuming ideal action of the smoothing capacitor $C$):

$$I_{SC,0} = I_{SC}$$

$$I_{SC,1} = I_{SC} \cdot D$$

The voltage across each SC bank will evolve according to the well known equation:
where \( C_{SC,1} \) are the equivalent capacitances in Farad of the two SC banks. 

From Fig. 2, we can write the voltage balance equation:

\[
V_{DC} = V_L + V_{HB} + V_{SC,0} \tag{6}
\]

Expressing the converter output voltage as function of the duty cycle \( D \), neglecting the energy stored in the inductor (SC energy is orders of magnitude higher), and assuming therefore the system to be almost always in dynamic steady state \[9\] during a charge/discharge cycle, the voltage balance reduces to:

\[
V_{DC} = D \cdot V_{SC,1} + V_{SC,0} \tag{7}
\]

Substituting (4) and (7) into (5), we can derive the differential equation relating the voltages across the two SC banks:

\[
V_{SC,1} \cdot dV_{SC,1} = C_{SC,0} \cdot (V_{DC} - V_{SC,0}) \cdot dV_{SC,0} \tag{8}
\]

Such equation can be solved for any given set of initial conditions \( V_{SC,0}(0) \) and \( V_{SC,1}(0) \):

\[
V_{SC,1}(t) = \sqrt{V_{SC,1}^2(0) + \frac{C_{SC,0}}{C_{SC,1}} \cdot 2(V_{DC} - V_{SC,0}(0)) \cdot \Delta V_{SC,0}(t) - \Delta V_{SC,1}^2(t)} \tag{9}
\]

with \( \Delta V_{SC,0}(t) = V_{SC,0}(t) - V_{SC,0}(0) \).

The most remarkable aspect of (9) is that the voltage (or, equivalently, the SOC) of the controlled SC bank \( V_{SC,1} \) is a unique function of the voltage of the uncontrolled bank \( V_{SC,0} \), and such a function does not depend on the particular shape of the converter output current. This fact allows us to design the SC banks so that they cycle between minimum and maximum voltage levels selectable by design. In particular, the following relationship holds:

\[
\frac{C_{SC,1}}{C_{SC,0}} = \left( \frac{V_{SC,0,Max} - V_{SC,0,Min}}{V_{SC,1,Max}^2 - V_{SC,1,Min}^2} \right) \tag{10}
\]

### B. Design for Optimal Energy Extraction

If the voltage at the terminal of a capacitive storage device of capacitance \( C_{SC} \) is allowed to vary between \( V_{SC,\text{min}} \) and \( V_{SC,\text{Max}} \), the amount of energy that can be cycled in and out from the device is:

\[
E_{SC,\text{cycle}} = \frac{1}{2} \cdot C_{SC} \cdot (V_{SC,\text{Max}}^2 - V_{SC,\text{min}}^2) \tag{11}
\]

Given the operational constraints (1) and (2), it makes sense to design the system with the aim of maximizing (11) for a given amount of total capacitance \( C_{SC} \). In the topology of Fig. 2, the maximum voltage across each SC bank is limited by (2) and by the voltage withstanding capabilities of SC banks and power devices in the half bridge. As a design starting point we will select:

\[
V_{SC,0,Max} = V_{SC,1,Max} = V_{DC} \tag{12}
\]

As it will be shown in a following chapter, the choice in (12) leads to a significant reduction of the VA ratings of the switches employed in the half bridge.

It is important to notice that, in terms of energy storage capability, the series connection of two capacitive banks of capacitance \( C_{SC,0} \) and \( C_{SC,1} \), each rated for a voltage \( V_{DC} \), is equivalent to a single bank rated for the same \( V_{DC} \) and having capacitance \( C_{SC} = C_{SC,0} + C_{SC,1} \).

In the proposed system, for a given amount of total system capacitance \( C_{SC} \) dictated by the application, the degree of freedom available for design is the capacitance ratio \( x = C_{SC,0} / C_{SC,1} \), and the function to be maximized is the relative energy extraction, defined as the ratio of the energy that can actually be cycled in and out from the SC banks and the total energy content of the banks:
Evaluating the banks’ minimum voltage from (10), taking the constraint (1) into account, the expression above can be written in terms of the design parameter \( x \), only:

\[
\frac{E_{SC, cycle}}{E_{tot}} = 0.5 \left( C_{SC, 0} \left( V_{SC, 0, min}^2 - V_{SC, 0, min}^2 \right) + C_{SC, 1} \left( V_{DC}^2 - V_{SC, 1, min}^2 \right) \right)
\]

\[
0.5 \left( C_{SC, 0} + C_{SC, 1} \right) V_{DC}^2
\]

The relative energy extraction is plotted in Fig. 4, showing that maximum extraction, equal to about 77%, is achieved for \( x = 2 \). The same figure also shows that any capacitance ratio between about 1.4 and 3 will allow for at least 75% energy extraction. In particular, the design corresponding to \( x = 3 \) is the one that had been suggested in [8], based on intuitive considerations; such a sub-optimal design corresponds to both SC banks being cycled between rated voltage and half of it, thus yielding exactly 75% energy extraction.

C. Volt-Ampere Rating of the Half Bridge Switches

In the converter of Fig. 2, the power electronics switches, when in the OFF state, have to be able to withstand a voltage equal to the maximum voltage of the SC bank behind the bridge. According to (12):

\[
V_{SW, rat} = V_{DC, SC, 0, max} = V_{DC}
\]

The maximum current that flows into the switches when they are in the ON state is equal to the inductor current:

\[
I_{SW, rat} = I_{SC, Max}
\]

Defining the power rating of the SC buffer system \( P_{Sw, rat} \) as the maximum power at the terminals connected to the DC link, we get the relationship between the VA rating of the switches and the buffer rated power:

\[
S_{SW, rat} = V_{SW, rat} \cdot I_{SW, rat} = V_{DC} \cdot I_{SC, Max} = P_{sw, rat}
\]

It is now possible to compare the proposed system with one based on a standard half bridge interface, as shown in Fig. 3. For a fair comparison, the same DC link voltage is assumed for the two systems. In this condition, the voltage rating of the switches is the same as in (15). In order to allow for at least 75% energy extraction at rated power, the current rating of the switches must be:

\[
I_{SW, rat} = I_{L, Max} = I_{SC, Max} \cdot \frac{V_{DC}}{V_{SC, min}} = 2 \cdot I_{SC, Max}
\]

The VA rating of each switch is therefore:

\[
S_{SW, rat} = V_{SW, rat} \cdot I_{SW, rat} = 2 \cdot V_{DC} \cdot I_{SC, Max} = 2 \cdot P_{sw, rat}
\]

Direct comparison of (17) and (19) shows that the system in Fig. 2 can be made out of switches having half VA rating compared to the system in Fig. 3.

III. SIMULATION OF THE IDEAL SYSTEM

In order to verify the correctness of the theory, and in particular the validity of (9) under arbitrary charge/discharge cycles, the system in Fig. 5 has been simulated using Simulink with Power System Blockset. In the simulation model, all components are supposed to be ideal and lossless. The current reference for the SC buffer, \( I_{SC, ref} \), is calculated from the load current \( I_{Load} \) according to the following law:

\[
I_{SC, ref} = \begin{cases} 
0 & \text{if } |I_{Load}| < I_{DC, Max} \\
I_{Load} - I_{DC, Max} & \text{if } |I_{Load}| \geq I_{DC, Max} 
\end{cases}
\]

The above control strategy is aimed at keeping the current from the DC source (most likely a battery) within the design limit \( \pm I_{DC, Max} \). If the load current exceeds such a limit, the excess current will be given (or absorbed) by the SC bank. In actual applications, the algorithm used to calculate the desired SC current can be more complex and will most likely involve other system parameters; however, the particular choice of \( I_{SC, ref} \) has no impact on the performance of the proposed system, and the simplified law (20) can be used to illustrate the cycling characteristics.

The inner current control used to track the reference \( I_{SC, ref} \)
is a standard PI loop; other controller structures are also possible, if better performance is deemed necessary.

Fig. 6 shows a cycle with a current profile of arbitrary shape and so that the SC banks undergo a complete discharge cycle, followed by a complete charge. The DC (battery) voltage is fixed to 150 V. The capacitances of the upper and lower banks are selected as 200 mF and 600 mF, respectively, resulting in $3x = \frac{200}{600} = 0.333$, and in a 50% maximum discharge of both banks, as predicted by (10). Both banks are initially “full”, meaning that their voltage is at the maximum bound, selected by design equal to the battery voltage (150 V).

As predicted by the theory, the SC banks can be cycled with arbitrary current shape and both blocks reach “depleted” and “fully charged” states simultaneously, effectively acting as a single SC bank. Notice that at the end of discharge the total SC voltage is exactly equal to the battery voltage and, due to (1), no further discharge is possible, resulting in 75% energy utilization.

The simulation is repeated in Fig. 7, for the same load current profile, the same initial conditions and the same total amount of energy storage, but with a capacitance ratio $x = 2$, resulting in $C_{SC,1} = 266.7 \text{ mF}$ and $C_{SC,0} = 533.3 \text{ mF}$.

Comparing the two simulations, it is possible to conclude that the two systems are equivalent from the point of view of the load (current profiles are identical); the individual SC bank voltages follow different trajectories, as predicted by (9). What is more important is that, at the end of discharge, the system with $x = 2$ still has not reached the discharge limit defined by (1), meaning that the SC banks can still give some energy to the load. This result was expected, since $x = 2$ had been shown to be the optimal design in terms of energy extraction capabilities.

IV. THE REAL SYSTEM AND NEED FOR DYNAMIC BALANCING

In a real system components will not be ideal. Battery, SCs, inductor and switches will all have their equivalent series resistance that will dissipate energy during charge/discharge cycles. This will cause the voltages across the two SC blocks to deviate from the ideal relationship (9). As an example, Fig. 8 shows the result of cycling the SC system with an unbalanced cycle where the energy required by the load exceed the capacity of the SC banks. In this case the bank is designed with $x = 3$, and the internal resistance of SCs (0.09Ω and 0.03Ω for upper and lower bank, respectively) is included in the simulation. At the end of each discharge cycle, the operating limit (1) is reached and the battery has to supply the load with no help from the SC buffer. During cycling, the voltage sharing between the two banks steadily deviates from the value predicted by (9), with the consequence of greatly reducing the system capability to store (and give back) energy; in fact, it can be noticed that after few cycles, the SC buffer is no longer able to absorb all the regenerative energy from the load and, from that point, the portion of the cycle in which the battery has to supply the load without any help from the SC buffer is getting larger at each cycle, effectively impairing the usefulness of the SC buffer.

The problem is solved by using a lossless equalization...
circuit [10] that continuously transfers energy between the banks in order to keep the individual voltages aligned with their theoretical values. The system is depicted in Fig. 9. Equalization of the proposed system is slightly more difficult than the standard equalization problem faced when series connecting many SC cells, since the instantaneous voltage of the two blocks must not be identical at all times; instead, the voltage of one block is a unique function of the other block voltage, as suggested by (9). The control method employed for voltage sharing is shown in Fig. 10, showing how the duty cycle of the balancing bridge $D_{bal}$ is calculated from the instantaneous voltage mismatch. The effectiveness of the strategy is proved by the simulation in Fig. 11, where the voltage across each SC block is shown under the same conditions as in the simulation of Fig. 8, but with the balancing circuit active. Diverging trend is removed and, as a consequence, the system is undergoing identical cycles with no deterioration of energy storage capabilities. Notice that the current involved in the equalization process is much lower than the main current $I_{sc}$, meaning that the equalization system does not significantly add to the overall system cost.

V. EXPERIMENTAL RESULTS

In order to validate the proposed concept, an experimental setup has been built, whose specifications are given in Table 1.

The two SC banks are made up of arrays of nominally identical elementary cells as shown in the table, realizing a capacitance ratio $\chi=3$; within each bank, passive voltage sharing is achieved by connecting a small resistance across each cell.

Fig. 12 shows experimental charge-discharge cycles of the system with arbitrary load current. According to (20), the share of the load current taken by the battery is limited to $\pm 2 \, A$, with the SC bank providing or accepting all the rest. Both SC banks are designed to charge and discharge between upper and lower limits of 12.75 $V$ and 6.375 $V$, respectively, as indicated by the dashed lines in the figure.

It is observed that in spite of the non-stiff battery voltage and of all the other non ideal components, the SC banks follow the predicted voltage trajectory, hitting the lower and upper voltage limits simultaneously. This is achieved with

![Fig. 9 – The system complete with lossless dynamic voltage balancing](image)

![Fig. 10 – Voltage balancing control system](image)

![Fig. 11 – Simulated cycles of a system ($\chi=3$) with losses in the SC banks, with active voltage balancing.](image)

![Fig. 12 – Experimental results; charge/discharge with arbitrary load current](image)

**Table I**

<table>
<thead>
<tr>
<th>MAIN SPECIFICATIONS OF THE EXPERIMENTAL SETUP</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Battery</strong></td>
</tr>
<tr>
<td>12V, 10Ah</td>
</tr>
<tr>
<td><strong>SuperCapacitor</strong></td>
</tr>
<tr>
<td>elementary cell</td>
</tr>
<tr>
<td>$ESR_{sc} = 3.2 , m\Omega$ (±25%)</td>
</tr>
<tr>
<td><strong>Uncontrolled SC bank</strong></td>
</tr>
<tr>
<td>175F, 15V</td>
</tr>
<tr>
<td><strong>Controlled SC bank</strong></td>
</tr>
<tr>
<td>58.3F, 15V</td>
</tr>
</tbody>
</table>

![Fig. 10 – Voltage balancing control system](image)

![Fig. 11 – Simulated cycles of a system ($\chi=3$) with losses in the SC banks, with active voltage balancing.](image)

![Fig. 12 – Experimental results; charge/discharge with arbitrary load current](image)
irregular behavior observed around non-ideal factors, including a non-stiff battery voltage. The balancing. As in simulation, the voltage drift is completely experimental system equipped with dynamic voltage indication of a system malfunction. The load current was done in the simulation of Fig. 8. The behavior of the system is very similar to the simulated one, with the voltage was temporarily switched from positive to negative due to a mistake of the operator and the system just followed the command.

very little current flowing through the lossless balancing circuit. From a system point of view, the two SC banks are behaving like a single bank being cycled between the voltage limits imposed by the design.

Fig. 13 shows the result of cycling the experimental system with a complete discharge, followed by a partial recharge, as it was done in the simulation of Fig. 8. The behavior of the system is very similar to the simulated one, with the voltage sharing between the two banks gradually diverging from the value predicted by (9) in the case of a lossless system.

VI. CONCLUSION

A method to interface a supercapacitor-based power buffer with a stiff DC source has been presented. It has been shown that the topology allows for independent control of the SC buffer current with more than 75% energy cycling capabilities; This is achieved by series connecting two banks of supercapacitors and by the use of only two solid state devices with half Volt-Ampere rating than what would be necessary if a conventional half bridge is employed.

Design guidelines for the proposed topology are given, showing that optimal energy extraction is obtained by using a capacitance ratio of 2, between the two series connected banks of supercapacitors.

Both simulations and experiments validate the principle, making the system attractive due to the lower converter cost and higher efficiency resulting from the use of lower rating power electronics devices. The use of a small and virtually lossless dynamic voltage balancing circuit, that is necessary to compensate for the losses in the components, allows for optimal energy extraction even if the DC link voltage is not stiff.

REFERENCES