Phase-Locked Loop with Adaptive Signal Cancellation for Three-phase Network Side Voltage Source Inverter

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Abstract
Circuits for synchronizing power converters to the three-phase utility voltages are often sensitive to voltage disturbances. Some kind of filtering device is needed. Voltage information is also important for system protection. Both voltage and frequency disturbances could be disadvantageous for the equipment. In this paper an alternative solution for improving the performance of a synchronizing circuit based on a phase-locked loop is proposed. It takes advantage of signal delay cancellation for calculating the symmetrical components of the three-phase voltages, but the delayed signal is estimated by an adaptive method. Other solutions for filtering input voltages are available, but they are mostly frequency dependent. The proposed solution is frequency independent. In addition, inherent signals may be utilized for protection purposes, since both instantaneous frequency and voltage values are estimated. This includes both positive and negative sequence voltages. The design has been simulated, and the simulation results are verified through experimental results.

Introduction
One of the major challenges connecting distributed power generation systems (DPGS) to the utility network, is their controllability. If the control system is not robust, this connection may lead to instability or failure. The DPGS should have a certain ride-through capability, to run over short grid disturbances [1].

Information about the grid voltages is needed, both in order to synchronize power converters and to control protective elements such as circuit breakers and the like. During severe faults, DPGS should be disconnected from the utility network, in order to avoid islanding and to protect equipment. Nevertheless, it would be beneficial if the disconnected DPGS could run in stand-alone operation until the grid voltages are restored.

Traditional devices for grid voltage synchronization and voltage disturbance detection often assume the grid frequency to be constant. If, however, parts of the distribution grid are weak, such devices may display a poor performance during frequency variations. The simplest circuits are also sensitive to voltage disturbances such as transients, harmonics and asymmetry.

A traditional phase-locked loop [2,3] is a common solution for generating a voltage synchronizing signal for the power converter, and it has inherent low-pass properties, thereby filtering out short voltage disturbances. However, it is sensitive to voltage asymmetry and harmonics and needs some
additional filtering. In [4] a multi-variable filter is proposed. This filter effectively removes both voltage harmonics and the 2\textsuperscript{nd} harmonic disturbance caused by voltage asymmetry. If the grid frequency is fluctuating, this filter design would both attenuate and phase shift the signals as soon as the frequency deviates from its nominal value.

A frequency change can be disastrous for specific kinds of equipment and should be carefully monitored. In [5], an adaptive and robust method is applied for fast frequency estimation. The method uses fast Fourier transform (FFT) and thereby requires a time consuming algorithm to produce a frequency estimate.

One way of monitoring the voltage condition for protection purposes, is to calculate the symmetric components of the three-phase voltages. A fast and simple way of doing this is described in [6], based on Delayed Signal Cancellation (DSC). In this method, signals have a fixed delay, determined by the grid frequency. If the frequency drifts from its nominal value, the performance of the method is deteriorated. In [6], the authors analyze the impact of frequency deviations.

One way of estimating the grid frequency is to take advantage of the inherent estimated angular frequency in the PLL. An adaptive signal cancellation (ACS) method is proposed in this paper. It both acts as a filter for the PLL and as a symmetric component voltage estimator for the protection devices. This adaptive solution has very good frequency tracking properties, and the design is robust. The design is realized in an field programmable gate array (FPGA) circuit, thereby obtaining very fast calculations and a compact design.

**System Description**

Fig. 1 shows the complete system. The input voltages $v_a$, $v_b$ and $v_c$ are converted into $v_\alpha$ and $v_\beta$ through the Clark-transform $abc/\alpha\beta$. The signal delay estimator calculates the signals $\hat{v}_\alpha$ and $\hat{v}_\beta$.

The phase sequence detector performs a DSC operation and a calculation of the amplitudes of the symmetric voltage components $|v_p|$ and $|v_n|$. The estimated positive sequence signals $v_{\alpha,p}$ and $v_{\beta,p}$ are put into the PLL, which returns estimated angular frequency $\omega$ and phase angle $\theta$, plus $\sin \theta$ and $\cos \theta$.

If the signals $v_\alpha$ and $v_\beta$ from the Clark-transform are connected directly to the PLL, the phase sequence detector will continue to estimate the symmetric voltage components, but the filtering properties of the ASC system will not be utilized.

**Phase-locked Loop**

Zero crossing voltage detection and the utilization of the quadrature of the input signals are two common techniques for realizing a PLL [2 - 4]. The first is very simple, but voltage information between the zero crossing points is not available.
The second solution, using the quadrature of the input signals, provides voltage information during the entire utility period. This method is more complicated and requires more computations.

In this work, the quadrature of the input signals was chosen. The diagram of the PLL is shown in fig. 2. In the lower parts of the figure, the input signals are multiplied with internal signals, as expressed in (1).

$$v_d = v_a \sin \hat{\theta} + v_\beta \cos \hat{\theta}$$

By keeping the reference value $v_{d,ref} = 0$, the synchronous reference voltage component $v_d$ is minimized, and thereby the PLL will remain locked to the input voltages $v_\alpha$ and $v_\beta$.

The transfer functions for the loop filter (LF) and the voltage controlled oscillator (VCO) are shown in (2) and (3), respectively. As can be seen, the loop filter is a PI controller, and the VCO is simply an integral.

$$H_{LF}(s) = k_p + \frac{k_i}{\tau_i s}$$

$$H_{VCO}(s) = \frac{1}{s}$$

**Signal Delay Estimator**

Fig. 3 shows the block diagram of the signal delay estimator. An important condition for this circuit to function, is that the reference angle $\theta$ is synchronized to the voltage signals $v_\alpha$ and $v_\beta$.

The two control loops in the top and the bottom of the figure amplifies the sine and cosine signals of $\theta$, until they have equal amplitude to the input signals. The transfer function of the closed loop is expressed by (4), and it acts as a first order low-pass filter.

$$H(s) = \frac{\frac{1}{\tau_{ASC,s}}}{1 + \frac{1}{\tau_{ASC,s}}} = \frac{1}{1 + \frac{1}{\tau_{ASC,s}}}$$

**Fig. 2: Block diagram of phase-locked loop**

**Fig. 3: Block diagram of signal delay estimator**
If the input signals have constant amplitudes, the integrators will eventually output the amplitudes of these signals. The feedback for the upper and lower control loop are expressed in (5) and (6), respectively,

\[
\dot{v}_a = V_a \cos \theta \\
\dot{v}_\beta = V_\beta \sin \theta
\]  

where \(V_a\) is the amplitude of \(v_a\) and \(V_\beta\) is the amplitude of \(v_\beta\). Then the output signals are expressed in (7) and (8).

\[
\dot{v}_{a,del} = V_a \sin \hat{\theta} \\
\dot{v}_{\beta,del} = -V_\beta \cos \hat{\theta}
\]

As long as the PLL is synchronized and the amplitudes \(V_a\) and \(V_\beta\) are consistent with the real values, the output signals will be lagging 90 degrees delayed to the input signals, for any utility voltage frequency. However, during step voltage changes the estimator will need some time to follow the input signal, due to the low-pass characteristic described in (4).

**Phase Sequence Detector**

This part of the design utilizes a traditional DSC method and is shown in fig. 4. The mathematical description is given in (9) and (10).

\[
\begin{align*}
\dot{v}_{a,p} &= \frac{1}{2}(v_a - \dot{v}_{\beta,del}) \\
\dot{v}_{\beta,p} &= \frac{1}{2}(v_\beta + \dot{v}_{a,del}) \\
\dot{v}_{a,n} &= \frac{1}{2}(v_a + \dot{v}_{\beta,del}) \\
\dot{v}_{\beta,n} &= \frac{1}{2}(v_\beta - \dot{v}_{a,del})
\end{align*}
\]

An additional circuit estimates the amplitudes of the output signals from the DSC circuit shown in fig. 4. The amplitudes are determined by using Park transforms with different synchronous references for the positive and the negative sequence system.

**Realization in FPGA**

The system described in fig. 1 was realized on an FPGA of type Xilinx Virtex 2. The clock frequency is 40 MHz, and the sampling frequency of the AD converters is 200kS/s. The FPGA board is placed in a LabView computer and is programmed by compiling LabView code to VHDL code. In [7], a solution is described where additional current and voltage controllers are included in the FPGA design.

By using an FPGA, one obtains very fast calculations and a structure with many parallel functions. The design is robust. FPGA cannot perform floating point calculations, and the multiplications need logic space. Sine and cosine calculations are solved by using look-up tables. Data is transferred between parallel functions by using FIFO registers.

**System Stability**

The proposed solution combines two adaptive systems, namely the PLL and the ASC circuit. They are interactive, and must be properly tuned, in order to obtain system stability. If the PLL has too fast
response, it may be disturbed by sudden changes in the output values of the ASC circuit. If the latter has too slow response, it will not effectively detect sudden voltage changes. By making the PLL slower and the ASC circuit faster, the system is stable.

Fig. 5 shows the control loop of the PLL, where V is the amplitude of the input voltage, k_p is the proportional gain, k_i is the integral gain, and τ_{PLL} is the time constant of the integrator. The transfer function for the closed loop is given in (11). Table 1 shows the chosen parameter values for the controllers.

\[ H_{PLL}(s) = \frac{\tau_{PLL} s + 1}{\tau_{PLL} s^2 + \tau_{PLL} s + 1} \]  

Table 1: Control parameters

<table>
<thead>
<tr>
<th>V</th>
<th>230</th>
</tr>
</thead>
<tbody>
<tr>
<td>k</td>
<td>0.0154</td>
</tr>
<tr>
<td>τ_{PLL}</td>
<td>0.01</td>
</tr>
<tr>
<td>τ_{ADC}</td>
<td>0.005</td>
</tr>
</tbody>
</table>

The Bode diagram for both systems is shown in fig. 6. The cutoff frequency for the PLL is chosen to be about 3 Hz, which should give sufficient response for common frequency variations on the grid. The tuning of the PLL is a trade-off between proper filtering and sufficient damping. The ASC circuit is tuned to give a fast response. Fig. 6 shows good margins between the PLL and the ASC circuit, margins which should be wide enough to provide system stability.

Fig. 6: Bode diagram for PLL and ASC
Simulation Results

A major voltage drop could be critical to the equipment, and a voltage drop exceeding 50% of nominal voltage, should be cleared in 160ms, according to [8]. The same applies to a voltage swell exceeding 120% of nominal voltage.

Some typical faults causing asymmetry are described in [9]. One of them is a single-line-to-ground fault (slg), where the phase voltage of one phase drops as a result of a ground fault. A line-to-line fault (ll) causes the phase voltage angles to move closer to each other, and the voltage drops in the power lines create a voltage drop in the affected phases. A line-to-line-to-ground fault (llg) causes a voltage drop in the affected phases. These arcing faults are shown in fig. 7.

Generators with a weak connection to the utility grid may show considerable rotor oscillation as a response to a disturbance, with a changing frequency as a result. This can be the case in distribution networks with a combination of wind power and hydro power. A sudden gust of wind can cause rotor oscillation in hydro power generators close to the wind farm. Voltage harmonics may also reduce the performance of distribution generation equipment, and the total harmonic distortion (THD) should be less than 8%, according to [10].

Simulations were done in Matlab/Simulink.

![Diagram of voltage sag and swell](image)

Fig. 7: Asymmetry caused by arcing faults. (a) single-line-to-ground fault, (b) line-to-line fault, (c) line-to-line-to-ground fault.

Voltage Sag and Swell

Fig. 8 shows simulation results of the above mentioned voltage disturbances. The low-pass characteristic of the signal delay estimator is the source of the apparent negative sequence signals immediately after the step changes. In fig. 8a and b it takes just 5ms for the positive sequence signal to cross the thresholds of 80% and 110% of nominal voltage, respectively.

![Simulation results of voltage sag and swell](image)

Fig. 8a: Voltage sag to 40% of nominal value. From the top: Phase voltage $v_a$, phase error, positive (solid) and negative (dashed) sequence voltage. The dash-dot line indicates 80% of nominal voltage. 

b: Voltage swell to 130% of nominal value. The dash-dot line indicates 110% of nominal voltage.
Voltage Asymmetry

In this case, the phase voltages of phase b and c are reduced to 75% of nominal voltage, and the voltages are phase shifted 30 degrees towards each other. The fault occurs at 5.0s and lasts for 0.5s.

Fig. 9 shows the performance of the circuit during these conditions. The phase voltage plot reveals that the voltage suddenly is phase shifted and decreased. The positive and negative sequence signals behave as expected.

Frequency Variation

The time variant angular frequency is defined in (12):

$$\omega(t) = 100\pi + 5e^{-0.2t} \sin(2t)$$  \hspace{1cm} (12)

where $\omega(t)$ is the angular frequency of the grid.

A comparison is made between the suggested design and the PLL proposed in [4]. Symmetrical voltages with nominal values are supplied for 10s, and the frequency changes as expressed in (13). Performance of estimated angle frequency and voltage reference angle are to be analyzed.

Fig. 10 shows the performance of the two different solutions. Since the multi variable filter is tuned at 50Hz, frequency deviations will cause significant phase displacement to occur. During normal operation (49.9 – 50.1Hz) this will not be a big problem, but fig. 10 reveals that any deviation from 50.0Hz will cause some phase displacement.

The solution proposed in this paper, on the other hand, is very nearly unaffected, since the filtering properties of the PLL is frequency independent.

Voltage Harmonics

In this case, the simulation starts with pure sinusoidal symmetrical voltages, and harmonics are introduced at 5.0s and remain for the rest of the simulation. The distorted voltages contain 10% fifth harmonics and 5% seventh harmonics, and this is done in order to go beyond the limits described in [10].

![Fig. 9: Line-to-line fault. From the top: Phase voltage $v_b$, phase error, positive (solid) and negative (dashed) sequence voltage.](image)

![Fig. 10: Frequency variation. From the top: Phase error: PLL with ASC (solid), PLL with multi variable filter (dashed); Frequency: Grid frequency (solid), estimated frequency from PLL with DSC (dashed), estimated frequency from PLL with multi variable filter (dashed-dotted).](image)
Fig. 11 shows that the PLL is influenced by the voltage distortions, and the cyclic deviation is less than one degree, with a period of 10ms. Total THD for $\sin \hat{\theta}$ and $\cos \hat{\theta}$ is 0.8% and 0.68%, respectively, during the distorted period.

The negative sequence signal has a mean value of about 12V with a 100Hz ripple. The positive sequence signal increases a bit, and also has, for this signal, a 100Hz ripple.

A circuit for identifying the harmonic content is not included, but it is feasible, as long as the harmonics are present in the unfiltered positive and negative sequence signals.

**Experimental Setup**

Fig. 12 shows the block diagram of the experimental setup. A voltage reference generator creates reference voltages with user-defined disturbances. These reference values are reproduced by an DC/AC converter with output filter, and the switching frequency is 10kHz. The filter is an LC-filter with a cutoff-frequency of 1kHz. The step up transformer is needed to bring the output voltage closer to the nominal voltage of the PLL with ADC circuit. The transformer is Yy0 connected.

Fig. 13 shows the setup on the lab. To the left is the computer with the reference generator and the PWM. The LC-filter is placed on the table close to the computer, and the DC source is partly hidden by an oscilloscope. The step up transformer is placed on the left part of the table, and the load resistance is placed on the floor below the table. The rack contains measurement equipment and a power converter, and a computer with the FPGA board included is placed on the top of the rack.

Fig. 11: Voltage harmonics. From the top: Phase voltage $v_a$, phase error, positive (solid) and negative (dashed) sequence voltage.

Fig. 12: Block diagram of the experimental setup

Fig. 13: Photo of the experimental setup
Voltage Sag and Swell

Fig. 14 a and b shows experimental results for voltage sag and swell, respectively. The plots display the positive and the negative sequence signals from the ASC circuit. The response is quite fast, and two small peaks in the negative sequence signals occur immediately after the step changes, as expected.

Fig. 14: a) Voltage sag to 80% of nominal value. b) Voltage swell to 120% of nominal value. Solid line: positive sequence component. Dashed line: negative sequence component.

Voltage Asymmetry and frequency variation

Fig. 15 shows the plot of a line-to-line fault. During the fault, the voltages of phase b and c are reduced by 35% and shifted 30 degrees. This severe asymmetry can be readily detected by the signal changes in fig. 15.

Fig. 16 shows a frequency variation with a maximum overshoot of 3Hz. The estimated frequency tracks the real frequency during the entire frequency disturbance. Some noise peaks appear on the signal, but the effect on the PLL would be negligible, according to (3). For control and protection purposes, this noise can be filtered out, if necessary.

Fig. 15: Line-to-line fault. 35% sag in phase b and c and 30 degrees phase shift. Solid line: positive sequence component. Dashed line: negative sequence component.

Fig. 16: Frequency variation Solid line: reference frequency. Dashed line: estimated frequency.
Finally, phase a was disconnected, and fig. 17 a and b shows the performance of the PLL without the ASC circuit and then with the ASC circuit. The filtering properties of the ASC improve the performance significantly, as can be seen from the plots.

Fig. 17: a) Reference angle $\theta$ without ASC. b) Reference angle $\theta$ with ASC.

**Conclusion**

The proposed solution for improving the performance of a synchronizing circuit takes advantage of DSC for calculating the symmetrical components of the three-phase voltages, by using an adaptive method called ASC. The proposed solution is frequency independent and provides signals for protection purposes, by estimating instantaneous frequency and voltage values. Simulations and experimental results validate the performance and robustness of the design. The proposed design is better than classical solutions for DPGS with weak grid connection.

**References**


[4] Benhabib M. C., Sadate S.: A New Robust Experimentally Validated Phase Locked Loop for Power Electronic Control, EPE Journal Vol 15 no 3, pp. 36- 48


