Analytical Power Loss Expressions for Diode Clamped Converters

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Keywords
Multilevel converters, Devices, Modeling.

Abstract
Use of multilevel converters has become popular the recent years for high power applications [1]. Numerous topologies have been introduced and investigated for utility and drive applications. For drive applications, the most popular topology seems to be the diode clamped topology introduced in [2]. When designing a converter it is useful to have analytically formulas to calculate electrical stresses in the switching devices at different loading. This paper is presenting analytical expressions for the power losses in the switching devices in 4- and 5-level diode clamped converters.

The equations derived in this paper are based on a method presented in [3] and [4]. It is a method to calculate the discontinuous currents in Pulse Width Modulated (PWM) converters with high switching frequency. The method transforms discontinuous currents or voltages to continuous, which are almost similar with respect to power losses.

By using analytical expressions, time consuming time domain simulations are avoided. At last a comparison of the switching and conduction losses between 2-, 3-, 4- and 5-level is done.

Basis for deriving the equations
The method samples the discontinuous current or voltage (Figure 1) within a switching interval, \( T_p \), and transforms it into a continuous microscopic mean or rms signal. Equation (1) shows the microscopic mean and rms current. By integrating the continuous microscopic mean or rms signal over a whole period, we can get a good approximation of the actual mean and rms value in a component, which is the macroscopic value. By sampling the current, \( i_f(\tau) \), in the middle of the switching interval and multiply with the duty ratio \( d(\tau) \) in each switching period we get the mean value of the current in a switching interval. When the switching frequency is high (typical > 10 times fund.), the current in one switching interval will change very little and the error will be small.

\[
i_{\tau, \text{avg}} = \frac{1}{T_p} \int_{a(\tau)/2}^{a(\tau)/2 + T_p} i_f(\tau) d\tau = d(\tau) i_f(\tau)
\]

\[
i_{\tau, \text{rms}} = \frac{1}{T_p} \int_{a(\tau)/2}^{a(\tau)/2 + T_p} i_f^2(\tau) d\tau = d(\tau) i_f^2(\tau)
\]

(1)
Figure 1: Current in a switch during a switching interval.

All the following derivation of equations and simulations are done with sinusoidal PWM. The modulation functions are

\[
\alpha_a = M \sin(\omega t)
\]
\[
\alpha_b = M \sin(\omega t - 2\pi / 3)
\]
\[
\alpha_c = M \sin(\omega t + 2\pi / 3)
\]

(2)

Where \( M \) is the amplitude modulation factor. The load currents are sinusoidal, given by

\[
i_a = \hat{I} \sin(\omega t - \varphi)
\]
\[
i_b = \hat{I} \sin(\omega t - 2\pi / 3 - \varphi)
\]
\[
i_c = \hat{I} \sin(\omega t + 2\pi / 3 - \varphi)
\]

(3)

The conducting voltage in semiconductors can be approximated as a forward voltage drop, \( U_F \), and an ohmic resistance, \( r_F \), in series with the forward voltage

\[
u_F = U_F + r_F \cdot i
\]

(4)

Thus, the conducting losses will be

\[
P_{\text{CON}} = \frac{1}{T_p} \int_{t_p} u_F \cdot i \ dt
\]

(5)

Inserting equation (4) and recognizing the formulas for mean and rms values of the discontinuous current gives

\[
P_{\text{CON}} = U_F \cdot I_{av} + r_F \cdot I_{rms}^2
\]

(6)

Where

\[
I_{av} = \frac{1}{T_p} \int_{t_p} i \ dt, \quad I_{rms}^2 = \frac{1}{T_p} \int_{t_p} i^2 dt
\]

(7)

A widely used way of calculating the switching losses in semiconductor devices is to utilize the switching energy emitted. The switching energy as a function of the current can be approximated to have a parabolic shape:
\[ e(i) = k_{1,T}i + k_{2,T}i^2 \]  \hfill (8)

Where \( k_{1,T} \) and \( k_{2,T} \) are constants of proportionality to be decided from the datasheet of the component. In this paper, the switching energy is approximated to have a straight line shape \((k_{2,T} = 0)\). This gives a good approximation within a specific area. Further, we obtain the switching losses in a component in an \( n \)-level converter, using the parabolic shaped switching energy:

\[ P_{SW} = \frac{U_d}{(n-1)} \frac{1}{2\pi} f_s \int (k_{1,T}i + k_{2,T}i^2) d\omega t \]  \hfill (9)

\( U_d \) is the DC link voltage and \( f_s \) is the triangular frequency (Figure 2). The integral limits will depend on the instants when the respective component switches. It should be mentioned that the inner clamping diodes in 4-level and 5-level converters would have some intervals in which they are switching but still have no switching losses. In these intervals there will not be any voltage across the clamping diodes, which implies that no switching losses will occur.

If this averaging should be acceptable, the switching period, \( T_p \), must be less than the thermal time constant for the semiconductor devices. In 4- and 5-level converters, the inner clamping diodes will also at some instants be exposed to a higher reverse voltage than the other components. However, at the intervals at which they are switching, they will all have the same reverse voltage applied: \( U_d/(n-1) \).

4-level converter

Each bridge leg consists of 6 switches in series as shown in Figure 2. It can easily be seen from Figure 2 that the instant where the top transistor in bridgeleg a starts its conducting interval will be where

\[ M \cdot \sin(\omega t) = \frac{1}{2} \Leftrightarrow \omega t = \arcsin\left(\frac{1}{2M}\right) \]  \hfill (10)

\[ \text{Figure 2: One phase leg of a 4- and 5-level converter (left), and their control signals (right).} \]

From (10), the expressions for the three duty ratio functions for bridge leg a and their validity intervals are derived

\[ d_{1a} = \begin{cases} 0, & 0 < \omega t < \arcsin\left(\frac{1}{2M}\right) \\ \frac{1}{2}M \sin(\omega t) - \frac{1}{2}, & \arcsin\left(\frac{1}{2M}\right) < \omega t < \pi - \arcsin\left(\frac{1}{2M}\right) \\ 0, & \pi - \arcsin\left(\frac{1}{2M}\right) < \omega t < 2\pi \end{cases} \]  \hfill (11)
These duty ratio functions describe how much of the switching period the three top IGBTs in bridge leg a are conducting. Depending on the load, the phase angle $\phi$ may operate in three different intervals, which gives different analytically expressions for the currents:

$$
0 < \omega t < \pi + \arcsin\left(\frac{1}{3M}\right) \\
\pi + \arcsin\left(\frac{1}{3M}\right) < \omega t < 2\pi - \arcsin\left(\frac{1}{3M}\right) \\
2\pi - \arcsin\left(\frac{1}{3M}\right) < \omega t < 2\pi
$$

Because of symmetry in the load currents, the losses in each bridge leg will be the same and hence, it is necessary to investigate only on leg. By investigation, $T_{x1+}$ and $T_{x3-}$ has identical current waveforms, only phase shifted $180^\circ$, thus the losses will be the same. This is also true for $T_{x2+}/T_{x2-}$ and $T_{x3+/T_{x1}}$. The freewheeling diodes $D_{x1+}/D_{x2+}/D_{x3+}$ share the same current waveform and are phase shifted $180^\circ$ to the currents in $D_{x1-}/D_{x2-}/D_{x3-}$. By the same argumentation, the losses in the clamping diodes $D_{x1}$ and $D_{x3}$ are equal, and also in $D_{x2}$ and $D_{x4}$.

As an example, the mean value of the current in $T_{a2+}/T_{a2-}$ in the interval $M>1/3$ and $\pi-\arcsin(1/(3M))<\phi<\pi$ will be:

$$
I_{avg} = \frac{1}{2\pi} \left( \int_{\phi}^{\pi+\arcsin(1/(3M))} d_{2a} \cdot i d\omega t + \int_{\pi+\arcsin(1/(3M))}^{\pi} d_{2a} \cdot i d\omega t \right)
$$

$$
= \frac{1}{12\pi} \left( \frac{\sqrt{9M^2-1}}{M} \cos(\phi) + 6 + 9\cos(\phi) \cdot M \cdot \arcsin\left(\frac{1}{3M}\right) \right)
$$

The formulas are verified by simulations in Saber with $f_s=1500\text{Hz}$. The verification where done over the modulation range $M = [0.2, 1]$ and $\phi = [-150^\circ, 150^\circ]$. The formulas had an error less than 0.5 % with respect to $I$. The worst case is for $T_{a2+}$ with $M = 1$ and $\phi = 0^\circ$, where the deviation between simulated and calculated current value was 0.74 A, for a load current of 100 A (rms).

### 5-level Converter

In the case of a 5-level converter, the instant where the top transistor in bridge leg a starts its conducting interval is:

$$
M \cdot \sin(\omega t) = \frac{1}{2} \Leftrightarrow \omega t = \arcsin\left(\frac{1}{2M}\right)
$$
From (16) we can obtain the expressions for the four duty ratio functions for bridge leg a and their validity intervals, with sine PWM:

\[
d_{1a} = \begin{cases} 
0, & 0 < \omega t < \arcsin\left(\frac{1}{3M}\right) \\
2M \sin(\omega t) - 1, & \arcsin\left(\frac{1}{3M}\right) < \omega t < \pi - \arcsin\left(\frac{1}{3M}\right) \\
0, & \pi - \arcsin\left(\frac{1}{3M}\right) < \omega t < 2\pi 
\end{cases}
\]

(17)

\[
d_{2a} = \begin{cases} 
1, & 0 < \omega t < \arcsin\left(\frac{1}{2M}\right) \\
2M \sin(\omega t), & \arcsin\left(\frac{1}{2M}\right) < \omega t < \pi - \arcsin\left(\frac{1}{2M}\right) \\
0, & \pi - \arcsin\left(\frac{1}{2M}\right) < \omega t < 2\pi 
\end{cases}
\]

(18)

\[
d_{3a} = \begin{cases} 
1, & \pi - \arcsin\left(\frac{1}{2M}\right) < \omega t < \pi \\
0, & 0 < \omega t < \pi - \arcsin\left(\frac{1}{2M}\right) \\
2M \sin(\omega t) + 1, & \pi - \arcsin\left(\frac{1}{2M}\right) < \omega t < 2\pi - \arcsin\left(\frac{1}{2M}\right) \\
0, & 0 < \omega t < \pi + \arcsin\left(\frac{1}{2M}\right) 
\end{cases}
\]

(19)

\[
d_{4a} = \begin{cases} 
0, & 0 < \omega t < \pi \\
2M \sin(\omega t) + 2, & \pi + \arcsin\left(\frac{1}{2M}\right) < \omega t < 2\pi - \arcsin\left(\frac{1}{2M}\right) \\
0, & 2\pi - \arcsin\left(\frac{1}{2M}\right) < \omega t < 2\pi 
\end{cases}
\]

(20)

As for the 4-level case, these duty ratio functions describe how much of the switching period the four top IGBTs in bridge leg-a are going to conduct. For the b- and c-phase, the duty ratio functions are shifted by \(2\pi/3\).

Depending on the load, the phase angle \(\phi\) may operate in three different intervals, just as for the 4-level topology. Because of symmetry in the load currents, the losses in each bridge leg will be the same and hence, it is necessary to investigate only on leg. By the same argumentation as for the 4-level converter, the losses in \(T_{x1+}/T_{x4-}\), \(T_{x2+}/T_{x3-}\), \(T_{x3+}/T_{x2-}\), \(T_{x4+}/T_{x1-}\), all the freewheeling diodes, clamping diodes \(D_{x1}/D_{x6}\), \(D_{x2}/D_{x5}\), \(D_{x3}/D_{x4}\) will be the same respectively.

Simulations in Saber with the same input data as for the 4-level topology were done to verify the formulas. The formulas had an error less than 1 %. The worst case is for the clamping diode \(D_{a3}\) with \(M = 0.6\) and \(\phi = 90^\circ\), where the deviation between simulated and calculated current value was 1.16 A for a load current of 100 A (rms).

**Comparison of different converters**

When a set of analytical expressions for the currents is established, the formulas can be put in a spreadsheet. Ratings for different loads and semiconductor devices can easily be analyzed, avoiding time consuming circuit simulations. As an example a 2-pole induction motor with a constant load torque of 3200 Nm can be used. The motor is assumed to draw a constant current, 458 A (rms), from the converters. The given value of \(\cos\phi\) is assumed to be at a constant 0.93, even though induced voltages will affect this value as the output frequency is varied between 0 to 50 Hz. Thus the results are not very accurate for low frequencies. The input DC-link voltage is assumed constant 2300 V. The output power from the converters at full speed is about 1 MW. The dc-bus capacitors are assumed to share this voltage equally. For simplicity reasons, one standard IGBT module is used for all the diodes and switches within one converter. This means that they will have the same rated voltage and current. As mentioned earlier, the inner clamp diodes in 4- and 5-level converters will be exposed to the highest reverse voltage. So either can all components be rated according to this voltage or else all components can be rated to \(V_\phi/(n-1)\), where \(n\) is the number of levels in the converter, and utilize
series connection of diodes for the inner clamping diodes. The chosen set of modules is listed in Table I. The results from the comparison are shown in Figure 3-Figure 5.

Table I: Modules used in the different converters [5].

<table>
<thead>
<tr>
<th>Topology</th>
<th>IGBT (Eupec)</th>
<th>Rated Voltage</th>
<th>Rated Current</th>
</tr>
</thead>
<tbody>
<tr>
<td>5-level</td>
<td>FF 800 R12 KL4C</td>
<td>1200 V</td>
<td>800 A</td>
</tr>
<tr>
<td>4-level</td>
<td>FF 800 R12 KL4C</td>
<td>1200 V</td>
<td>800 A</td>
</tr>
<tr>
<td>3-level</td>
<td>FZ 800 R17 KF6B2</td>
<td>1700 V</td>
<td>800 A</td>
</tr>
<tr>
<td>2-level</td>
<td>FZ 800 R33 KF2</td>
<td>3300 V</td>
<td>800 A</td>
</tr>
</tbody>
</table>

Figure 3: Total conduction losses in the different converters at $f_s=1$kHz.

Figure 4: Total switching losses in the different converters at $f_s=1$kHz.

1200V devices is used for both the 4- and 5-level converter (Table I). 600V devices can not be used for a 5-level topology at this dc-bus voltage (2300V). This is favorable for the 4-level converter compared to the 5-level regarding losses. With the same switching- and conduction loss parameters, the 4-level topology is superior to the 5-level, especially regarding the conduction losses (Figure 3), because of the less number of equal devices. With a lower dc-bus voltage, and use of 600V Devices, the 5-level topology would have achieved better utilization of the devices, and thus lower losses.
Figure 5: Total power losses in the different converters at $f_s=1$kHz. Right plot is normalized to the losses in the 2-level topology.

Conclusion

By this examination, it is shown that it is possible to derive analytically equations for both 4- and 5-level diode clamped converters. Through simulations with Saber, it is shown that the method gives good accuracy for pulse number higher than 10 times the fundamental. The sets of formulas are very helpful when the cooling system of the converter is to be designed. Comparison of different topologies is eased because time consuming simulations are avoided. With the device-, motor and converter ratings in this paper, the 4-level topology has the lowest overall losses (approx. 40% of the losses in the 2-level topology).

References